Power Estimation
Welcome

- If you are new to FPGA design, this module will help you estimate your FPGA power consumption.
- These design techniques promote fast and efficient FPGA design development.
After completing this module, you will be able to:

- List the three phases of the design cycle where power calculations can be performed
- Estimate power consumption by using the XPower Estimator spreadsheet
- Estimate power consumption by using the XPower software utility
Power Consumption Overview

- As devices get larger and faster, power consumption goes up
- First-generation FPGAs had
  - Lower performance
  - Lower power requirements
  - No package power concerns
- Today’s FPGAs have
  - Much higher performance
  - Higher power requirements
  - Package power limit concerns
  - A System Monitor that provides active monitoring of the die temperature
    - Refer to the Virtex-6 User Guide for more information
Power Consumption Concerns

- High-speed and high-density designs require more power, leading to higher junction temperatures

- Package thermal limits exist
  - 125°C for plastic
  - 150°C for ceramic

- Power directly limits
  - System performance
  - Design density
  - Package options
  - Device reliability
Estimating Power Consumption

- Estimating power consumption is a complex calculation
  - Power consumption of an FPGA is almost exclusively dynamic
  - Power consumption is dependent on design and is affected by
    - Output loading
    - System performance (switching frequency)
    - Design density (number of interconnects)
    - Design activity (percent of interconnects switching)
    - Logic block and interconnect structure
    - Supply voltage
Estimating Power Consumption

- Power calculations can be performed at three distinct phases of the design cycle
  - **Concept phase**: A rough estimate of power can be calculated based on estimates of logic capacity and activity rates
    - Use the Xilinx Power Estimator spreadsheet
  - **Design phase**: Power can be calculated more accurately based on detailed information about how the design is implemented in the FPGA
    - Use the XPower Analyzer
  - **System Integration phase**: Power is calculated in a lab environment
    - Use actual instrumentation

- Accurate power calculation at an early stage in the design cycle will result in fewer problems later
Activity Rates

- Accurate activity rates (also known as toggle rates) are required for meaningful power calculations.

- Clocks and input signals have an absolute frequency.

- Synchronous logic nets use a percentage activity rate:
  - 100% indicates that a net is expected to change state on every clock cycle.
  - Allows you to adjust the primary clock frequency and see the effect on power consumption.
  - Can be set globally to an average activity rate on groups or individual nets.

- Logic elements also use a percentage activity rate:
  - Based on the activity rate of output signals of the logic element.
  - Logic elements have capacitance.
Excel spreadsheets with power estimation formulas built in
- Enter design data in white boxes
- Power estimates are shown in gray boxes

Sheets
- Summary (device totals)
- Clock, Logic, I/O, Block RAMs, DSP, MMCM
- GTX, TEMAC, PCIE

To download go to http://www.support.xilinx.com -> Technology Solutions -> Power
- Download the XPE spreadsheet for your device family
  - XPE is not installed with the ISE software
- The Power Solutions page has numerous resources
Xilinx Power Estimator

Summary and Quiescent power

- White boxes allow you to enter design data
- Gray boxes show you the Power estimates
- Tabs at bottom allow you to enter power information per device resources (not shown)
- Settings reviews device, system, and environment information
- On-Chip Power breaks the estimated power consumption into device resources
Xilinx Power Estimator

- **Summary and Quiescent power**
  - Power Supply reviews what power sources will be necessary
  - Summary describes your systems total power and estimated junction temperature

![Power Supply Table]

![Summary Table]
### Xilinx Power Estimator

#### Clock power

<table>
<thead>
<tr>
<th>Name</th>
<th>Frequency (MHz)</th>
<th>Type</th>
<th>Fanout</th>
<th>Clock Buffer Enable</th>
<th>Slice Clock Enable</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock_a</td>
<td>100.0</td>
<td>Global</td>
<td>1000</td>
<td>100%</td>
<td>50%</td>
<td>0.010</td>
</tr>
<tr>
<td>clock_b</td>
<td>200.0</td>
<td>Global</td>
<td>1000</td>
<td>100%</td>
<td>50%</td>
<td>0.020</td>
</tr>
<tr>
<td>clock_c</td>
<td>250.0</td>
<td>Global</td>
<td>4000</td>
<td>100%</td>
<td>50%</td>
<td>0.053</td>
</tr>
<tr>
<td></td>
<td>0.0</td>
<td>Global</td>
<td>0</td>
<td>100%</td>
<td>50%</td>
<td>0.000</td>
</tr>
</tbody>
</table>

#### Logic power

<table>
<thead>
<tr>
<th>Name</th>
<th>Clock (MHz)</th>
<th>Logic</th>
<th>Shift Registers</th>
<th>Distributed RAMs</th>
<th>FFs</th>
<th>Toggle Rate</th>
<th>Average Fanout</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ctrl_block</td>
<td>200.0</td>
<td>2000</td>
<td>100</td>
<td>100</td>
<td>2000</td>
<td>12.5%</td>
<td>3.00</td>
<td>0.023</td>
</tr>
<tr>
<td>messenger_block</td>
<td>100.0</td>
<td>1000</td>
<td>0</td>
<td>0</td>
<td>1000</td>
<td>12.5%</td>
<td>3.00</td>
<td>0.005</td>
</tr>
<tr>
<td>state_machine</td>
<td>250.0</td>
<td>150</td>
<td>0</td>
<td>0</td>
<td>1250</td>
<td>12.5%</td>
<td>3.00</td>
<td>0.008</td>
</tr>
</tbody>
</table>

#### I/O power

<table>
<thead>
<tr>
<th>Name</th>
<th>I/O Standard</th>
<th>Input Pins</th>
<th>Output Pins</th>
<th>Bidir Pins</th>
<th>IO LOGIC SERDES</th>
<th>IO DELAY</th>
<th>IBUF LOW PWR</th>
<th>Clock (MHz)</th>
<th>Toggle Rate</th>
<th>Data Rate</th>
<th>Output Enable</th>
<th>Output Load (pF)</th>
<th>On Chip Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>control_outputs</td>
<td>LVCMOS 2.5V 12mA (Slow)</td>
<td>0</td>
<td>80</td>
<td>0</td>
<td>No</td>
<td>Off</td>
<td>Yes</td>
<td>100.0</td>
<td>12.5%</td>
<td>SDR</td>
<td>100.0%</td>
<td>0</td>
<td>0.001</td>
</tr>
<tr>
<td>processor_outputs</td>
<td>LVCMOS 2.5V 12mA (Slow)</td>
<td>0</td>
<td>50</td>
<td>0</td>
<td>No</td>
<td>Off</td>
<td>Yes</td>
<td>150.0</td>
<td>12.5%</td>
<td>SDR</td>
<td>100.0%</td>
<td>0</td>
<td>0.001</td>
</tr>
<tr>
<td>communicator</td>
<td>LVCMOS 2.5V 12mA (Slow)</td>
<td>0</td>
<td>100</td>
<td>0</td>
<td>No</td>
<td>Off</td>
<td>Yes</td>
<td>200.0</td>
<td>12.5%</td>
<td>SDR</td>
<td>100.0%</td>
<td>0</td>
<td>0.002</td>
</tr>
</tbody>
</table>
### Block RAM, DSP, and MMCM power

<table>
<thead>
<tr>
<th>Name</th>
<th>BRAMs</th>
<th>Mode</th>
<th>Toggl Rate</th>
<th>Clock (MHz)</th>
<th>Enable Rate</th>
<th>Bit Width</th>
<th>Write Mode</th>
<th>Write Rate</th>
<th>Clock (MHz)</th>
<th>Enable Rate</th>
<th>Bit Width</th>
<th>Write Mode</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory_bank_a</td>
<td>6</td>
<td>RAMB18</td>
<td>50.0%</td>
<td>100.0</td>
<td>25.0%</td>
<td>1 WRITE_FIRST</td>
<td>50.0%</td>
<td>0.0</td>
<td>25.0%</td>
<td>1 WRITE_FIRST</td>
<td>50.0%</td>
<td>0.001</td>
<td></td>
</tr>
<tr>
<td>memory_bank_b</td>
<td>10</td>
<td>RAMB18</td>
<td>50.0%</td>
<td>150.0</td>
<td>25.0%</td>
<td>1 WRITE_FIRST</td>
<td>50.0%</td>
<td>0.0</td>
<td>25.0%</td>
<td>1 WRITE_FIRST</td>
<td>50.0%</td>
<td>0.003</td>
<td></td>
</tr>
<tr>
<td>memory_bank_c</td>
<td>10</td>
<td>RAMB18</td>
<td>50.0%</td>
<td>200.0</td>
<td>25.0%</td>
<td>1 WRITE_FIRST</td>
<td>50.0%</td>
<td>0.0</td>
<td>25.0%</td>
<td>1 WRITE_FIRST</td>
<td>50.0%</td>
<td>0.004</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>DSP Slices</th>
<th>Clock (MHz)</th>
<th>Toggle Rate</th>
<th>MREG Used?</th>
<th>MULT Used?</th>
<th>Pre-add Used?</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter</td>
<td>4</td>
<td>250.0</td>
<td>12.5%</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>0.003</td>
</tr>
<tr>
<td>Transform</td>
<td>4</td>
<td>200.0</td>
<td>12.5%</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>0.002</td>
</tr>
<tr>
<td>Multiplier</td>
<td>6</td>
<td>100.0</td>
<td>12.5%</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>0.002</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Clock (MHz)</th>
<th>Phase Shift</th>
<th>Divide Counter</th>
<th>Multiply Counter</th>
<th>Clock 0 Divide</th>
<th>Clock 1 Divide</th>
<th>Clock 2 Divide</th>
<th>Clock 3 Divide</th>
<th>Clock 4 Divide</th>
<th>Clock 5 Divide</th>
<th>Clock 6 Divide</th>
<th>V_CCINT (W)</th>
<th>V_CC_AUX (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock_a</td>
<td>100.0</td>
<td>None</td>
<td>1</td>
<td>2</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>0.001</td>
<td>0.044</td>
</tr>
<tr>
<td>clock_b</td>
<td>150.0</td>
<td>None</td>
<td>1</td>
<td>1</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>0.001</td>
<td>0.042</td>
</tr>
<tr>
<td>clock_c</td>
<td>200.0</td>
<td>None</td>
<td>1</td>
<td>1</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>off</td>
<td>0.001</td>
<td>0.045</td>
</tr>
</tbody>
</table>
Xilinx Power Estimator

Graphs

- Power by Function
- Power over Vccint
- Power Variance: Process, Voltage, and Temperature
- Power over Temperature
What is the XPower Analyzer?

A utility for estimating the power consumption and junction temperature of FPGA and CPLD devices.

Reads an implemented design (NCD file) and timing constraint data.

You supply activity rates:
- Clock frequencies
- Activity rates for nets, logic elements, and output pins
- Capacitive loading on output pins
- Power supply data and ambient temperature
- Detailed design activity data from simulation (VCD file)

The XPower Analyzer calculates the total average power consumption and generates a report.
Running the XPower Analyzer

- Expand **Implement Design → Place & Route**
- Double-click **XPower Analyzer** to launch the XPower utility in interactive mode
- Use the **Generate Power Data** process to create reports using VCD files or TCL scripts

![Process Properties - XPower Analyzer Properties](image)
Summary

- Estimated junction temperature
- Reporting, settings, and thermal information is all placed in one utility
  - As you manipulate system characteristics you will update the generated report
- Report Navigator allows for quick migration to various reports and functions of the utility
Report Navigator

- Thermal Information
- Voltage Source Information
- Settings
- Each box is color coded
Produced as a simple text file
- File is given .pwr extension
- Report is more detailed and stored in one text file
- Some what-if analysis information is included
- Includes a Power Improvement Guide

<table>
<thead>
<tr>
<th>Power summary</th>
<th>I (mA)</th>
<th>P (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total estimated power consumption</strong></td>
<td></td>
<td>779.51</td>
</tr>
<tr>
<td>Total Vccint</td>
<td>1.00V</td>
<td>664.51</td>
</tr>
<tr>
<td>Total Vccaux</td>
<td>2.50V</td>
<td>12.00</td>
</tr>
<tr>
<td>Total Vcc25</td>
<td>2.50V</td>
<td>1.00</td>
</tr>
<tr>
<td>___</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clocks</td>
<td></td>
<td>0.00</td>
</tr>
<tr>
<td>DSP</td>
<td></td>
<td>0.00</td>
</tr>
<tr>
<td>IO</td>
<td></td>
<td>0.00</td>
</tr>
<tr>
<td>Logic</td>
<td></td>
<td>0.00</td>
</tr>
<tr>
<td>Signals</td>
<td></td>
<td>0.00</td>
</tr>
<tr>
<td>___</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Vccint</td>
<td>1.00V</td>
<td>664.51</td>
</tr>
<tr>
<td>Quiescent Vccaux</td>
<td>2.50V</td>
<td>12.00</td>
</tr>
<tr>
<td>Quiescent Vcc25</td>
<td>2.50V</td>
<td>1.00</td>
</tr>
<tr>
<td>___</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package power limits, ambient 55C</td>
<td></td>
<td>1801.96</td>
</tr>
<tr>
<td>250 LPM</td>
<td></td>
<td>2715.16</td>
</tr>
<tr>
<td>500 LPM</td>
<td></td>
<td>3070.18</td>
</tr>
<tr>
<td>750 LPM</td>
<td></td>
<td>3333.33</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thermal summary</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Estimated junction temperature</td>
<td>53C</td>
</tr>
<tr>
<td>θ airflow of 250 LPM</td>
<td>53C</td>
</tr>
<tr>
<td>500 LPM</td>
<td>53C</td>
</tr>
<tr>
<td>750 LPM</td>
<td>53C</td>
</tr>
<tr>
<td>Ambient temp</td>
<td>55C</td>
</tr>
<tr>
<td>Case temp</td>
<td>53C</td>
</tr>
<tr>
<td>θj-A</td>
<td>4°C/W</td>
</tr>
<tr>
<td>___</td>
<td></td>
</tr>
<tr>
<td>Max ambient at junction max of</td>
<td>85°C / 82°C</td>
</tr>
<tr>
<td>250 LPM</td>
<td>82°C</td>
</tr>
<tr>
<td>500 LPM</td>
<td>82°C</td>
</tr>
<tr>
<td>750 LPM</td>
<td>82°C</td>
</tr>
</tbody>
</table>
What Next?

- If you have a problem with your thermal budget there are many things you can consider
  - Determine which components in your design are using the most power
    - Try to use as much of the dedicated hardware as possible
  - Review the Power Improvement Guide section in the Advanced Power Report
  - Evaluate your activity rates
  - Reduce excess signal power or excess device utilization
    - Synthesis options
    - Implementation tool options
    - HDL code
    - Reduce excess static power
    - Adjust the external environment
Summary

- Power calculations can be performed at three distinct phases of the design cycle:
  - Concept phase: (Power Estimator spreadsheet)
  - Design phase: (XPower Analyzer)
  - System integration phase: (Lab measurements)

- Accurate power calculation at an early stage in the design cycle will result in fewer problems later.

- The Power Estimator spreadsheet and the XPower Analyzer can be used for estimating the power consumption and the junction temperature of all Xilinx FPGA and CPLD devices.

- The Power Estimator and XPower Analyzer uses activity rates to calculate total average power consumption.
Where Can I Learn More?

- Command Line Tools User Guide: XPower chapter
- Online help from the XPower GUI
- Xilinx Power Solutions Web Page
  - www.support.xilinx.com → Technology Solutions → Power Solutions
  - Get the XPower Estimator spreadsheets for all Xilinx devices
  - 7 Steps to Worst Case Power Estimation, WP353
  - Spartan-6 Power Management User Guide, UG394
  - Power Consumption at 40 and 45 nm, 298
- Application Notes: Help → Xilinx on the Web → Xilinx Application Notes
  - Application Note XAPP158: Powering Xilinx FPGAs
- Xilinx Training
  - www.xilinx.com/training
    - Xilinx tools and architecture courses
    - Hardware description language courses
    - Basic FPGA architecture and other topics (free training videos)
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