FPGAs-3
Design Without and With Constraints
Logic Placement Can Be Very Different

Without global timing constraints
Logic is placed randomly

With global timing constraints
Logic is placed close each other
Logic is placed to result in a faster design
Setup and hold time

• **Setup time:** The data must become valid at least a setup time before the arrival of the active clock edge at its pin.

• **Hold Time:** The data must stay valid at least a hold time after the arrival of the active clock edge at its pin.
Period Constraints

Cover Paths Between Synchronous Elements
PERIOD Constraint

Use the Most Accurate Timing Information

✓ Clock skew between the source and destination flip-flops
✓ Synchronous elements clocked on the negative edge
✓ Unequal clock duty cycles
✓ Clock input jitter
Period Constraint

Clock uncertainty is automatically accounted for in global constraint calculations

Clock jitter is a form of clock uncertainty
Period Constraint

Timing Analyzer calculation accounts for most accurate timing information.

Equation takes into account data path delay, clock skew and clock uncertainty.
PERIOD Constraint
Calculation takes into account inverted clock edges

- Assume:
  - 50 percent duty cycle on CLK
  - PERIOD constraint of 10 ns
  - Because FF2 will be clocked on the falling edge of CLK, the path between the two flip-flops will be constrained to 50 percent of 10 ns = 5 ns
Offset Constraints

Constrains I/O Pads To/From Synchronous Elements relative to associated clock signal.
Offset Constraints
Accounts for Clock Delay

- OFFSET IN = T_data_In - T_clk_In
- OFFSET OUT = T_data_Out + T_clk_Out
Offset Constraints

Timing Analyzer calculation accounts for most accurate timing information

**Slack**: 1.307 ns (requirement - (data path - clock path - clock arrival + uncertainty))

Equation takes into account clock path, clock arrival, and clock uncertainty.
PERIOD Constraint Options

- TIMESPEC name
- Specific constraint value
  - Active clock edge
  - Duty cycle
- Relative to other PERIOD TIMESPEC
  - Useful for designs with multiple clock signals
  - Can define both frequency and phase relationships
- Input jitter
Entering OFFSET Constraints

- Global OFFSET IN and OFFSET OUT constraints can be made from Inputs or Outputs
- Right-click here and select **Create Constraint** to make an OFFSET constraint
Access the Constraints Editor

Enter constraints in the Constraints Editor GUI

- Expand **User Constraints** in the Processes for Source window
- Double-click **Create Timing Constraints**
NET "clk" TNM_NET = clk;
TIMESPEC TS_clk = PERIOD "clk" 20 ns HIGH 50%;
OFFSET = IN 7 ns VALID 20 ns BEFORE "clk" RISING;
OFFSET = OUT 7.5 ns AFTER "clk";
TIMESPEC TS_clk1_to_clk2 = FROM clk1 TO clk2 8 ns;
Constrain from time group clkA to time group clkB to be 8 ns.
Pad to Pad Constraints

Covers Purely Combinatorial Paths that start and end at I/O pads

TIMESPEC TS_Pad2Pad = FROM PADS TO PADS 14.4 ns;
Latches

• Level-sensitive storage
  – Data transmitted while enable is '1'
    • *transparent* latch
  – Data stored while enable is '0'

![Latch Diagram]

![Waveform Diagram]