Homework #6

Start assignment as soon as possible. Work individually, but you can ask your classmates for help when you get stuck without sharing any code. Please send me email if something isn't clear and I will update the assignment.

Notes:

- Clearly state whether your design is fully functional, and state the failing sections if any exist.
- Make sure your design and code are easily readable and understandable (clear and well commented).
- For all problems, perform the required test(s) and submit a table printed by your verilog testbench module listing all inputs and corresponding outputs,

Keep “hardware” modules separate from testing code. Instantiate a copy of your processing module(s) in your testing module (the highest level module) and drive the inputs and check the outputs from there.
1. **Repeat of HW4 problem 1 with Vivado**
   Design a circuit that compute the product of 128 element-vectors, a and b; that is a vector p such that \( p_i = a_i * b_i \). The elements of a and b are stored in separate SSRAMS and the result is to be written into a third SSRAM. Assume that computation is started by a control signal, \( \text{go} \) being one during a clock cycle and output control signal, \( \text{done} \) is to be set to one during the cycle when the computation is complete. Assume a and b are 16-bit values.

**Implementation**

i. For the design make sure you register the inputs and outputs, and add timing constraint for the clock and report the design speed using post Place and Route Static Timing Analysis (under Place and Route). Slack must be a minimum positive number (near zero). Report slack (set-up and hold time if available) and design speed. If design couldn’t make the timing constraint, slow down the clock until it meets the timing.

ii. Perform Synthesis and Place and Route and report total slice count, and other major FPGA resource counts that are listed in Summary Report.

iii. Using the Power analyzer tool, report the power dissipation of the design for your clock specification that design can operate.
2. **Repeat of HW4 problem 2 with vivado**
   This problem was explained in the class: Design a FIFO to store up to 256 data items of 16-bits each, using 256x 16-bit dual-port SSRAM for the data storage. Assume the FIFO will not be read when it is empty, not to be written when it is full, and that the write and read ports share a common clock.

**Implementation**

i. For the design make sure you register the inputs and outputs, and add timing constraint for the clock and report the design speed using post Place and Route Static Timing Analysis. Slack must be a minimum positive number (near zero). Report slack (set-up and hold time if available) and design speed. If design couldn’t make the timing constraint, slow down the clock until it meets the timing.

ii. Perform Synthesis and Place and Route and report total slice count, and other major FPGA resource counts that are listed in Summary Report.

iii. Using the Power analyzer tool, report the power dissipation of the design for your clock specification that design can operate.