Homework #5

Start assignment as soon as possible. Work individually, but you can ask your classmates for help when you get stuck without sharing any code. Please send me email if something isn't clear and I will update the assignment.

Notes:

- Clearly state whether your design is fully functional, and state the failing sections if any exist.
- Make sure your design and code are easily readable and understandable (clear and well commented).
- For all problems, perform the required test(s) and submit a table printed by your verilog testbench module listing all inputs and corresponding outputs,

Keep “hardware” modules separate from testing code. Instantiate a copy of your processing module(s) in your testing module (the highest level module) and drive the inputs and check the outputs from there.
1. [25 pts] The purpose of this problem is to familiarize you with the synthesis and place and route process and to give you a rough feeling for the size of a few simple circuits. Turn in a detailed report with the results for each part.

   o For all designs register the inputs and outputs, and add timing constraint for the clock (e.g 500 MHz=2ns). Report slack (set-up and hold time if available). If it couldn’t make the timing constraint, slow down the clock until it meets the timing.

   o Synthesize and place and route the following blocks and report their total slice count, and other FPGA resource counts that are listed in Summary Report (this includes all logic utilization numbers under Device Utilization Summary). Include registers (flip-flops) and constrain the timing path as explained in the class. Assume words are all 2’s complement signed unless stated otherwise. No need to simulate, only turn in the source verilog, but your verilog must compile correctly (Use “Check Syntax” in Synthesis flow).

   o Report delay for each block using Place and Route Static Timing Analysis (under Place and Route). Slack must be a minimum positive number (zero or near zero e.g 0.1 ns).

   o Using the XPower analyzer tool (under Place and Route), report the power dissipation of each block for your clock specification that the design can operate. Note that for power number, your design clk must be set to the number that you found in previous step, and place and route must be done again.

   o Report results for all circuits in a table. Report the numbers in a single table so it can be used as a note sheet in the future.

   o Include verilog files for each circuit in the report.

Blocks

   a) [15 pts] two input 10-bit adder (11-bit output). Use "$+$" in verilog.

   b) [20 pts] 16-bit x 16-bit unsigned multiplier (32-bit output). Use "$\ast$" in verilog with two different options

      i. Make the synthesis use LUT for implementation and report timing, slice count and power results

      ii. Make the synthesis use Multiplier Blocks for implementation and report timing, slice count and power results
2. [40 pt] Repeat the same steps in Problem 1 for your memory multiplier in HW4 problem 2 to fully place and route the design and report these items:
   i. Report maximum clk that the design can achieve by adding timing constraints and minimum slack timing.
   ii. Report total slice count, and other FPGA resource counts from
   iii. Report the power consumption at the frequency that it can work
   iv. Do all these steps for your Verilog-based design and IP core-based design