CURRICULUM VITAE

Tinoosh Mohsenin

Assistant Professor
Director of Energy Efficient High Performance Computing (EEHPC) Lab
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Google Scholar Citations:1153, h-index:16, i10-index:27

Education

Ph.D.	11/2010	University of California, Davis, CA, Electrical and Computer Engineering
M.S.	05/2003	Rice University, Houston, TX Computer Engineering
B.S.	05/1999	Sharif University of Technology, Tehran, Iran Electrical Engineering

Professional Experience

01/2011-present	University of Maryland, Baltimore County, Baltimore, MD Assistant Professor, CSEE Department
09/2002-11/2010	University of California Davis and Rice University Graduate Research Assistant
05/2002 –08/ 2002	Nokia Research Center, Irving, TX Summer intern

Awards and Honors

Best Paper Award-Honorary Mention IEEE 50th ISCAS Conference, May 2017

Best Paper Award-Honorary Mention, Neural Systems and Applications Technical Committee of IEEE Circuits and Systems Society, May 2017

National Science Foundation (NSF) CAREER Award, March 2017

Best Paper Award ACM GLSVLSI Conference, May 2016

Nominated for Best PhD Dissertation Award, 2011

External Funding

Total External Funded Grants: $1.48M, My Share: $1M
I have been Principal Investigator (PI) for most of my funded grants.

National Science Foundation (**PI),** AWARD #1652703 Title: "CAREER: DeepMatter: A Scalable and Programmable Embedded Deep Neural Network, Total: $475,104, 05/01/2017-04/31/2022

National Science Foundation (**PI),** #1652703 Title: "NSF Student Travel Grant for 2017 IEEE International Symposium on Circuits and Systems (ISCAS)", I am local arrangement chair for the 50th

IEEE ISCAS conference, with over 1000 participants and this grant is a new initiative for supporting US students to travel and present at ISCAS this year. Total: $30,000, 05/01/2017-10/31/2017

Lockheed Martin (Co-PI, Collaborative), Title: "Radio Frequency Signal Classification Using Deep Neural Networks", Total: $125,000, My share: $41,600, 09/01/2016-12/31/2017

Army Research Lab (PI, Collaborative) "Online, Adaptive Artifact Identification for Real World Neuroimaging: Algorithms and Hardware", Total: $246,392, My share: $123,96, 08/01/2016-04/31/2018

National Science Foundation (PI, UMBC Lead in Multi-campus-Collaborative) AWARD#1526913, Title: "CSR: Small: Collaborative Research: A Heterogeneous Ultra Low Power Accelerator for Wearable Biomedical Computing", Total $500,000, My share: $ 211,976, 09/01/2015-08/31/2018

National Science Foundation (PI): AWARD#1350035, Title: "EAGER: Multi-physiological Signal Processing Architectures for Seizure Detection", Total: $99,803, Oct. 2013- Dec. 2016

Boeing Corporation Foundation (PI): $10,000, September 2015-present

National Science Foundation CNS (Senior Personnel): Title: "MRI: Acquisition of Cutting-Edge GPU and Phi Nodes for the Interdisciplinary UMBC High Performance Computing Facility", $605,850, 07/15/2017-07/14/2020

Equipment Support from Industry

Boeing Corporation (PI): Server and desktop, gift with total value of $5500, April 2017

NVIDIA Corporation (PI): GPU Tesla P40 and boards, gift with total value of $7000, April 2017

Xilinx Corporation (PI): Software, gift with total value of $13,198, July 2013, September 2014

Xilinx Corporation (PI): FPGA boards, gift with total value of $3,495, July 2013

Internal Funding

UMB-UMBC Seed Grant (PI, Collaborative Multi-campus), Title: "Wearable Multimodal System for Monitoring of Epilepsy Patients", Total $50,000, My share: $25,000. 03/20/2015-08/20/2017

Students

Total of 7 PhD and 14 MS students and one Postdoc have worked under my supervision in the EEHPC Lab. Two PhD and 9 MS students graduated under my supervision.

Postdoctoral Researcher

Siamak Aram, Postdoctoral Research Associate, "EEG Data Analysis for Brain Functions and Activities", (PhD, Politecnico di Torino, Italy, 2015), August 2017-present

Ph.D. Students

PhD Completed, Primary Advisor

1. Adam Page, December 2016, Senior Engineer at SamTech Inc.
   Dissertation Title: "Deploying Deep Neural Networks in Embedded Real-Time Systems".
2. Amey Kulkarni, February 2017, Senior R&D Engineer at Velodyne LiDAR Inc.
   Dissertation Title: "Heterogeneous and Scalable Sketch-based Framework for Big Data Acceleration on Low Power Embedded Cores".

PhD in Progress, Primary Advisor

3. Ali Jafari, in progress, PhD Proposal Jan 2017, Dissertation November 2017, Chair
   Dissertation Title: "An Embedded Multi-Modal Deep Neural Network Processor for Time Series Data Classification".

4. Colin Shea, in progress, PhD Proposal November 2017, Chair
   Dissertation Title: "Scalable Deep Neural Networks for Real-time Low Power Applications".
5. Asmita Korde, in progress, PhD Proposal November 2017, Chair
   Dissertation Title: "Compressive Sensing for Gravitational Microlensing".
6. Morteza Hosseini, in progress, Chair
7. Rashidul Islam, in progress, Chair

PhD Committee Member

1. Qinglei Meng, PhD Proposal Aug 2017, Member
2. Ahmed Shahin, PhD Dissertation Apr 2017, Member
3. Brice Cannon, PhD Dissertation Apr 2015, Member
4. Tanvir Mahmood, PhD Dissertation Sept 2015, Member
5. Robert Schultz, PhD Dissertation Apr 2014, Member

Master's Students

MS Completed, Primary Advisor

1. Tahmid Abtahi, July 2017, Senseonics Inc. Thesis title: "Accelerating Convolutional Neural Network with FFT on Embedded Hardware".
2. Nasrin Attaran, April 2017, Thesis title: "Architecture Exploration for Low-Power Wearable Stress Detection".
3. Sri Harsha Konuru, August 2017, Project title: "An EEG Artifact Identification Embedded System using ICA and Multi-Instance Learning".
4. Abhilash Puranik, June 2017, Project title: "Embedded Low-Power Processor Analysis for Stress Detection".
5. Emily Smith, Dec. 2015, NSA, Project title: "The Design and Implementation of a Scalable Bus-based Cluster with Shared Memory for a Programmable Many-Core Platform".
6. Chris Sagedy, Dec.2015, NSA, Project title: "Development of an Architecture Simulator for the EEHPC Many-Core Processor".
7. Sina Viseh, August 2014, Thesis title: "A Low Power On-board Processor for a Tongue Assistive Device".
8. Asmita Korde, July 2013, NASA, Thesis title: "Detection Performance and Computational Complexity of Radar Compressive Sensing for Noisy Signals".
9. Darin Chandler, May 2012, Thesis title: "An Efficient Network on Chip Targeted to a Parallel, Low Power, Low-area Homogenous Many-Core DSP Platform".

MS in Progress, Primary Advisor

10. Adwaya Kulkarni, in progress, Chair
11. Lahir Marni, in progress, Chair
12. Chetan Thalisetty, in progress, Chair
13. Nathanael Buswel, in progress, Chair
14. Varun Sivasubramanian, in progress, Chair

MS Committee Member

1. Sushmita Kadiyala Rao, July 2011, Member
2. Yatish Joshi, Dec 2011, Member
3. Anush Chandrasekaran, July 2012, Member
4. Ahmad Abbas, July 2012, Member
5. Ajay Kallianpur, August 2012, Member
6. Neha Sardesai, Sept 2013, Member
7. Jeff turner, Feb 2014, Member
8. Sidharth Allani, Dec 2014, Member

Undergraduate Students

BS in Progress Primary Research Mentor

8.Yeerfan Tuerdi, March 2017-present, URA research mentor

BS Completed, Primary Research Mentor

7. Elise Donker, Apr 2015-May 2016, URA research mentor
6. Vignesh Dhanasekaran, Sept 2014-May2015, Research Mentor
5. Kamal Broomes, May 2013-May 2014, Research Mentor
4. Alec Pulianas, May 2013-May 2014 URA research mentor
3. Paul Boudra May 2012-May 2013, Research Mentor
2. Julian Field May 2012-May 2013, URA research mentor
1.Adam Page May 2012-Dec 2012, URA research mentor

Publications

***Note: I have underlined my student coauthors in my publications. Multiple author papers where I am the last author are published by my research group under my supervision**
Currently, total 18 Journals published/accepted and 3 in review. Total 45 peer reviewed conference articles published/accepted.

Peer-Reviewed Journal Articles

In Review Journals

J20. Tahmid Abtahi, Colin Shea, Amey Kulkarni, and **Tinoosh Mohsenin**, "Accelerating Convolutional Neural Network with FFT on Embedded Hardware", IEEE Transactions on Circuits and Systems I: Regular Papers (TVLSI), In review

Published/ Accepted Journals

J18. Page, Adam, Kulkarni, Adwaya, Attaran, Nasrin, Jafari, Ali, Mallik, Maria, Homayoun, Houman **Mohsenin, Tinoosh**, "A Low Power Manycore Accelerator for Personalized Biomedical Applications" IEEE Transactions on Very Large Scale Integration Systems, 12 pages, accepted August 2017. Impact Factor:1.7

J17. Ali Jafari, Nathanael Buswell, Maysam Ghovanloo, and **Tinoosh Mohsenin** "A Low Power Wearable Tongue Drive System for People with Severe Disabilities" IEEE Transactions on Biomedical Circuits and Systems, 11 pages, accepted August 2017. **Impact Factor: 2.95**

J16. M Hajkazemi, M. Khavari, **Tinoosh Mohsenin**, Houman Homayoun, "Heterogeneous HMC+DDRx Memory Management for Performance-Temperature Trade-offs". ACM Journal on Emerging Technologies in Computing Systems (JETC), 22 pages, accepted June 2017. Impact Factor: 1.4

J15. Amey Kulkarni, Colin Shea, Tahmid Abtahi and **Tinoosh Mohsenin**, "Low Overhead CS-based Heterogeneous Framework for Big Data Acceleration", ACM Transaction on Embedded Computing Systems (TECS), accepted May 2017, 25 pages, Impact Factor: 1.2

J14. Amey Kulkarni and **Tinoosh Mohsenin**, "Low Overhead Architectures for OMP Compressive Sensing Reconstruction Algorithm", In IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), Volume 99, 2017 pp.1-13, doi: 10.1109/TCSI.2017.2648854, 13 pages, **Impact Factor: 2.4**

J13. Adam Page, Colin Shea, **Tinoosh Mohsenin**, "SPARCNet: A Hardware Accelerator for Efficient Deployment of Sparse Convolutional Networks", In ACM Journal on Emerging Technologies in Computing Systems (JETC), Volume. 13, Issue 3, May 2017, Article No. 31, 32 pages, Impact Factor: 1.4

J12. Amey Kulkarni, Youngok Pino, Matthew French and **Tinoosh Mohsenin**, "Real-Time Anomaly Detection Framework for Many-Core Router through Machine Learning Techniques", In ACM Journal of Emerging Technologies in Computing Systems (JETC), Volume 13 Issue 1, Article 10, 22 pages, June 2016. Impact Factor: 1.4

J11. Adam Page, Chris Sagedy, Emily Smith, Nasrin Attaran, Tim Oates and **Tinoosh Mohsenin**, "A Flexible Multi-channel EEG Feature Extractor and Classifier for Seizure Detection", IEEE Transactions on Circuits and Systems-II, vol. 62, no. 2, pp. 109–113, Feb 2015. Impact Factor: 1.7

J10. Sina Viseh, Maysam Ghovanloo, and **Tinoosh Mohsenin**, "Towards an Ultra Low Power On-board Processor for Tongue Drive System", IEEE Transactions on Circuits and Systems-II, vol. 62, no. 2, pp. 174–178, Feb 2015. Impact Factor: 1.7

J9. Cannon, B.M.; Mahmood, T.; Astar, W.; Boudra, P.; **Mohsenin, T.**; Carter, G.M., "Polarization-Insensitive Phase-Transmultiplexing and Multicasting of CSRZ-OOK and 4 × RZ-BPSK to 4 × RZ-QPSK via XPM in a Birefringent PCF", IEEE Photonics Journal , vol.6, no.2, pp.1-11, April 2014 doi: 10.1109/JPHOT.2014.2309642. **Impact Factor: 2.3**

J8. B. M. Cannon, T. Mahmood, W. Astar, P. Apiratikul, G. Porkolab, P. Boudra, **T. Mohsenin**, C. J. K. Richardson, and G. M. Carter "All Optical Amplitude-Phase Transmultiplexing of RZ-OOK and RZ-BPSK to RZ-QPSK by Polarization-Insensitive XPM using a Nonlinear Birefringent AlGaAs Waveguide", Optics Express Journals, August 2013. **Impact Factor: 3.3**

J7. **Tinoosh Mohsenin**, Houshmand Shirani-Mehr and Bevan Baas, "LDPC Decoder with an Adaptive Wordwidth Datapath for Energy and BER Co-optimization", In Hindawi Transactions of VLSI Design, Article ID 913018, 12 pages, January 2013 (Acceptance rate: 21%)

J6. **Tinoosh Mohsenin**, Dean Truong and Bevan Baas, "A Low Complexity Message Passing Algorithm for Reduced Routing Congestion in LDPC Decoders", in IEEE Transactions of Circuits and Systems I, vol. 57, no. 5, pp. 1048–1061, May 2010, **Invited.**

J5. **Tinoosh Mohsenin** and Bevan Baas, "A Split-Decoding Message Passing Algorithm for Low Density Parity Check Codes," in Springer Journal of Signal Processing, vol. 61, issue 3, pp. 329–345, February 2010.

J4. Dean N. Truong, Wayne H. Cheng, **Tinoosh Mohsenin**, Zhiyi Yu, Anthony T. Jacobson, Gouri Landge, Michael J. Meeuwsen, Christine Watnik, Anh T. Tran, Zhibin Xiao, Eric W. Work, Paul V. Mejia, Bevan M. Baas, "A 167-Processor Computational Platform in 65 nm CMOS," in IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 4, pp. 1130-1144, April 2009, **Invited**.

J3. Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Dean Truong, **Tinoosh Mohsenin**, Bevan Baas, "AsAP: An Asynchronous Array of Simple Processors," in IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 3, pp. 695-705, March 2008.

J2. Ryan Apperson, Zhiyi Yu, Michael Meeuwsen, **Tinoosh Mohsenin**, Bevan Baas, "A Scalable Dual-Clock FIFO for Data Transfers between Arbitrary and Haltable Clock Domains," IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol. 15, no. 10, pp. 1125-1134, October 2007.

J1. Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, **Tinoosh Mohsenin**, Dean Truong, Jason Cheung, "AsAP: A Fine-grain Multi-core Platform for DSP Applications," IEEE Micro, vol. 27, no. 2, March/April 2007, **Invited.**

Peer-Reviewed Conference Proceedings

Published/Accepted

C47. Ali Jafari, Maysam Ghovanloo, and **Tinoosh Mohsenin**, "An Embedded FPGA Accelerator for a Stand-alone Dual-Mode Assistive Device", In Proceedings of IEEE Biomedical Circuits and Systems (BioCAS) Conference, 4 pages, Oct. 2017.

C46. Abtahi,Tahmid, Kulkarni, A., **Mohsenin, T.**. "Accelerating Convolutional Neural Network with FFT on Tiny Cores". In Proceedings of the 50th IEEE International Symposium on Circuits and Systems (ISCAS). May 2017, 4 pages, **Best Paper Award-Honorary Mention, Invited for TCAS-I journal.**

C45. Adwaya Kulkarni, Tahmid Abtahi, Colin Shea, Amey Kulkarni and **Tinoosh Mohsenin** "PACENet: Energy Efficient Acceleration for Convolutional Network on Embedded Platform", In Proceedings of the 50th IEEE International Symposium on Circuits and Systems (ISCAS), USA, May 2017, 4 pages, **Invited**.

C44. Jafari, A., Gandhi, S., Konuru, S. H., Hairston, W. D., Oates, **Tinoosh Mohsenin**, "An EEG Artifact Identification Embedded System using ICA and Multi-Instance Learning". In Proceedings of the 50th IEEE International symposium on circuits and systems (ISCAS). May 2017, 4 pages, **Invited.**

C43. Ali Jafari, Maysam Ghovanloo, and **Tinoosh Mohsenin**, "A Real-time Embedded FPGA Processor for a Stand-alone Dual-Mode Assistive Device " In Proceedings of the 25th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017, 1 page.

C42. Morteza Hosseini, Rashidul Islam, Amey Kulkarni and **Tinoosh Mohsenin** "A Scalable FPGA-based Accelerator for High-Throughput MCMC Algorithms" In Proceedings of the 25th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017, 1 page.

C41. Amey Kulkarni, Colin Shea, Houman Homayoun, and **Tinoosh Mohsenin**, "LESS: Big Data Sketching and Encryption on Low Power Platform", In proceedings of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE 2017), April 2017, 6 pages, Acceptance Rate: 24%

C40. Maria Malik, Katayoun Neshatpour, **Tinoosh Mohsenin**, Avesta Sasan and Houman Homayoun,, "Big vs Little Core for Energy-efficient Hadoop Computing", In proceedings of IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE 2017), April 2017, 6 pages, Acceptance Rate: 24%

C39. Nasrin Attaran, Justin Brooks and Tinoosh Mohsenin, " A Low-Power Multi-Physiological Monitoring Processor for Stress Detection ", In Proceedings of the IEEE sensors conference , October 2016, pp. 1-3.

C38. Adam Page, Colin Shea, and **Tinoosh Mohsenin**, "Wearable Seizure Detection using Convolutional Neural Networks with Transfer Learning". In Proceedings of 49th IEEE International Symposium Circuits and Systems (ISCAS), Montreal, Canada, May 2016, 4 pages, Acceptance Rate: 49%, **Invited.**

C37. Amey. Kulkarni, Ali. Jafari, Chris. Sagedy and **Tinoosh Mohsenin**, "Sketching-based High-Performance Biomedical Big Data Processing Accelerator", In Proceedings of 49th IEEE International Symposium Circuits and Systems (ISCAS), Montreal, Canada, May 2016, 4 pages, Acceptance Rate: 49%, **Invited.**

C36. Adam Page, Nasrin Attaran, H. Homayoun and **Tinoosh Mohsenin,** "Low-Power Manycore Accelerator for Personalized Biomedical Applications", In Proceedings of 26th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2016, pp. 63-68, 6 pages, Acceptance Rate: 27%, **Best Paper Award.**

C35. Amey Kulkarni, Tahmid Abtahi, Emily Smith and **T. Mohsenin**, "Low Energy Sketching Engines on Many-Core Platform for Big Data Acceleration", in Proceedings of the 26th ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 57-62, May 2016, 6 pages, Acceptance Rate: 27%.

C34. A. Page and **T. Mohsenin**. "FPGA-Based Reduction Techniques for Efficient Deep Neural Network Deployment". In Proceedings of IEEE 24th International Symposium Field-Programmable Custom Computing Machines (FCCM), May 2016, 1 page.

C33. Amey Kulkarni, Ali Jafari, Colin Shea, and **Tinoosh Mohsenin,** "CS-based Secured Big Data Processing on FPGA", In Proceedings of 24th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2016, 1 page.

C32. Amey Kulkarni, Youngok Pino and **Tinoosh Mohsenin,** "Adaptive Real-time Trojan Detection Framework through Machine Learning", In Proceedings of IEEE International Symposium on Hardware Oriented Security and Trust (HOST), May 2016, 4 pages, Acceptance Rate: 40%.

C31. Amey Kulkarni, Youngok Pino, **Tinoosh Mohsenin**, "SVM-based Real-Time Hardware Trojan Detection for Many-Core Platform", In proceedings of 17th IEEE International Symposium on Quality Electronic Design (ISQED), March 2016, 6 pages, Acceptance Rate: 36%.

C.30 Adam Page, Siddharth Pramod, Tim Oates, and **Tinoosh Mohsenin** "An Ultra Low Power Feature Extraction and Classification System for Wearable Seizure Detection", In proceedings of 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Milan, Italy, August 2015., 4 pages, **Invited.**

C29. Ali Jafari, Adam Page, Chris Sagedy, Emily Smith, **Tinoosh Mohsenin**,"A Low Power Seizure Detection Processor Based on Direct Use of Compressively-Sensed Data and Employing a Deterministic Random Matrix", In Proceedings of IEEE Biomedical Circuits and Systems (BioCAS) Conference, Oct. 2015, 4 pages.

C28. Adam Page and **Tinoosh Mohsenin**. "Utilizing deep neural nets for an embedded ECG-based biometric authentication system", In Proceedings of IEEE Biomedical Circuits and Systems (BioCAS) Conference, Oct 2015, 4 pages.

C27. Amey Kulkarni and **Tinoosh Mohsenin**, "Accelerating Compressive Sensing Reconstruction OMP Algorithm with CPU, GPU, FPGA and Domain Specific Many-Core", In Proceedings of the 48th IEEE International Symposium on Circuits and Systems (ISCAS'15), Lisbon, Portugal, May 2015, 4 pages.

C26. **Tinoosh Mohsenin** and Adam Page, "Towards A Low Power Wearable Personalized Seizure Detection System" In Proceedings of the IEEE EMBS Brain Grand Challenges, Nov 2014, 4 pages.

C25. Mohammad Khavari Tavana, Amey Kulkarni, Abbas Rahimi, **Tinoosh Mohsenin**, and Houman Homayoun, "Energy-efficient mapping of biomedical applications on domain-specific accelerator under process variation", In Proceedings of the 14'th IEEE International Symposium on Low Power Electronics and Design (ISLPED '14), 6 pages, Acceptance Rate: 34%.

C24. A. Kulkarni, Houman Homayoun and **Tinoosh Mohsenin** "A Parallel and Reconfigurable Architecture for Efficient OMP Compressive Sensing Reconstruction", In Proceedings of the 24'th ACM Annual Great Lakes Symposium on VLSI (GLSVLSI'2014), 6 pages, Acceptance Rate: 24%.

C23. Adarsh Reddy Ashammagari, Hamid Mahmoodi, **Tinoosh Mohsenin**, and Houman Homayoun. 2014. Reconfigurable STT-NV LUT-based functional units to improve performance in general-purpose processors", In proceedings of the 24'th Annual Great Lakes Symposium on VLSI (GLSVLSI'2014), 6 pages, Acceptance Rate: 24%.

C22. A. Page, JT Turner, **T. Mohsenin** and T. Oates, "High Resolution Multichannel Electroencephalography Data Analysis and Processing in Seizure Detection" In proceedings of The 27th International Conference of the Florida Artificial Intelligence Society (FLAIRS'27), May 2014, 4 pages,

C21. Brice Cannon; Tanvir Mahmood, William Astar, Paul Boudra,**Tinoosh Mohsenin** and Gary Carter "Polarization-Insensitive Phase-transmultiplexing of CSRZ-OOK and RZ-BPSK to RZ-QPSK via XPM in a PCF" In Proceedings of the 40th IEEE Optical Fiber Communication Conference (OFC), March 2014.

C20. Adam Page and **Tinoosh Mohsenin**, "An Efficient & Reconfigurable FPGA and ASIC Implementation of a Spectral Doppler Ultrasound Imaging System", In proceedings of the 24th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 24), June 2013.

C19. Jordan Bisasky, Houman Homayoun, Farhang Yazdani and **Tinoosh Mohsenin**, "A 64-core platform for biomedical signal processing", In proceedings of 14th IEEE International Symposium on Quality Electronic Design (ISQED), March 2013, 6 pages, Acceptance Rate: 27%.

C18. J. Stanislaus and **T. Mohsenin**, "High performance compressive sensing reconstruction hardware with QRD process," In proceedings of the 45th IEEE International Symposium on Circuits and Systems (ISCAS'12), May 2012

C17. J. Bisasky, J. Chander, and **T. Mohsenin**, "A many-core platform implemented for multi-channel seizure detection," In proceedings of the 44th IEEE International Symposium on Circuits and Systems (ISCAS'12), May 2012

C16. J. Stanislaus and **T. Mohsenin**, "Low-complexity FPGA implementation of compressive sensing reconstruction," In proceedings of The IEEE International Conference on Computing, Networking and Communications, (ICNC'13), January 2013

C15. James Darin Chandler, Jordan Bisasky, Jerome L.V.M. Stanislaus and **Tinoosh Mohsenin** "Real-time Multi-channel Seizure Detection and Analysis Hardware," In proceedings of The IEEE Biomedical Circuits and Systems Conference (BIOCAS '11), November 2011

C14. Houshmand Shirani-mehr, **Tinoosh Mohsenin** and Bevan Baas "A Reduced Routing Network Architecture for Partial Parallel LDPC Decoders," In proceedings of The Asilomar Conference on Signals, Systems and Computers (ACSSC'11), November 2011.

C13. **Tinoosh Mohsenin**, Houshmand Shirani-Mehr and Bevan Baas, "Low Power LDPC Decoder with Efficient Stopping Scheme for Undecodable Blocks", In proceedings of the 44'th IEEE International Symposium on Circuits and systems (ISCAS '11), May 2011, **Invited**.

C12. **Tinoosh Mohsenin** and Bevan Baas, "Trends and Challenges in LDPC Hardware Decoders," In proceedings of The Asilomar Conference on Signals, Systems and Computers (ACSSC), November 2009, pp. 1273–1277, **Invited**.

C11. **Tinoosh Mohsenin**, Dean Truong and Bevan Baas, "An Improved Split-Row Thresholding Decoding Algorithm for LDPC Codes," In proceedings of The IEEE International Conference on Communications (ICC'09), June 2009.

C10. **Tinoosh Mohsenin**, Dean Truong, and Bevan Baas, "Multi-Split-Row Threshold Decoding Implementations for LDPC Codes," In proceedings of The 42nd IEEE International Symposium on Circuits and systems (ISCAS '09), pp. 2449-2452, May 2009.

C9. **Tinoosh Mohsenin**, Pascal Urard and Bevan Baas, "A Thresholding Algorithm for Improved Split-Row Decoding of LDPC Codes," In proceedings of Asilomar Conference on Signals, Systems and Computers (ACSSC'08), pp. 448-451, October 2008.

C8. Dean Truong, Wayne Cheng, **Tinoosh Mohsenin**, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor Computational Array for Highly-Efficient DSP and Embedded Application Processing," In Proceedings of the HotChips Symposium of High-Performance Chips, (HotChips 2008), August 2008.

C7. Dean Truong, Wayne Cheng, **Tinoosh Mohsenin**, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling," In Proceedings of the IEEE Symposium on VLSI Circuits, pp. 22-23, June 2008.

C6. **Tinoosh Mohsenin** and Bevan Baas, "An 18 Gbps 2048-bit 10GBASE-T Ethernet LDPC Decoder", IEEE International Solid-State Circuits Conference (ISSCC) 2008 Student Research Forum, February 2008.

C5. **Tinoosh Mohsenin**, Bevan M. Baas, "High-throughput LDPC Decoders Using A Multiple Split-Row Method," In Proceedings of the 32nd International Conference on Acoustics, Speech, and Signal Processing (ICASSP'07), vol.2, pp. II-13-16, April 2007.

C4. **Tinoosh Mohsenin**, Bevan M. Baas, "Split-Row: A Reduced Complexity, High Throughput LDPC Decoder Architecture," In Proceedings of the IEEE International Conference of Computer Design (ICCD '06), pp. 320-325, October 2006.

C3. Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Daniel Gurman, Chi Chen, Jason Cheung, Dean Truong, **Tinoosh Mohsenin**, "Hardware and Applications of AsAP: An Asynchronous Array of Simple Processors," In Proceedings of the IEEE HotChips Symposium on High-Performance Chips (HotChips 2006), August 2006.

C2. Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, **Tinoosh Mohsenin**, Mandeep Singh, Bevan M. Baas, "An Asynchronous Array of Simple Processors for DSP Applications," In Proceedings of the IEEE International Solid-State Circuits Conference, (ISSCC '06), pp. 428-429, February 2006.

C1. Patrick Murphy, J. Patrick Frantz, Eric Welsh, Ricky Hardy, **Tinoosh Mohsenin** and Joseph Cavallaro, "VALID: Custom ASIC Verification and FPGA Education Platform," Microelectronic Systems Education Conference, (MSE'03), pp. 64-65, June 2003.

Peer Reviewed Workshops
Other Peer Reviewed Short Papers and Conference Presentations

A8. Adam Page, **Tinoosh Mohsenin,** "Accelerating Convolutional Neural Networks in Resource-Bound, Real-Time Embedded Systems", 2017 IEEE Design Automation Conference (DAC-WIP) Work-in-Progress Session, June 2017.

A7. Ali Jafari, Nathanael Buswell, Adam Page, Maysam Ghovanloo, and **Tinoosh Mohsenin** "A Low Power Wearable Tongue Drive System for People with Severe Disabilities" In 2016 International Solid-State Circuits Conference (ISSCC-SRP), Research Preview, January 2016.

A6. Asmita Korde-Patel, Barry, R.K., **Mohsenin, T**. "Application of Compressive Sensing to Gravitational Microlensing Data and Implications for Miniaturized Space Observatories". In proceedings of Astronomical Data Analysis Software and Systems (ADASS) Conference, 2016 National Inst. for Astrophysics Astronomical Observatory (INAF). Astronomical Society of the Pacific (ASP) Conference Series, Oct 2016

A5. Asmita Korde-Patel, Barry, R.K., **Mohsenin, T "**Application of Compressive Sensing to Gravitational Microlensing Experiments", IAU Symposium 325 on Astroinformatics. Cambridge University Press, Sept 2016.

A.4. Ali Jafari, Sina Viseh, Adam Page, Maysam Ghovanloo, and **Tinoosh Mohsenin** "An Ultra Low Power Tongue Drive System for Paralyzed Patients" In IEEE 2015 Strategic Conference on Healthcare Innovations and Point-of-Care Technologies for Precision Medicine, November 2015.

W6. A.Kulkarni and **T. Mohsenin** "High Performance Architectures for OMP Compressive Sensing Reconstruction Algorithm" in Proceedings of The 39th Annual GOMACTech Conference, April 2014, acceptance rate for oral presentation: 22%.

W5. S.Viseh, A.Acevedo, M. Ghovanloo and **T. Mohsenin** "Towards A Low Power FPGA Implementation for A Stand-Alone Intraoral Tongue Drive System" in Proceedings of The 39th Annual GOMACTech Conference, April 2014, acceptance rate for oral presentation: 22%

W4. JT Turner, A. Page, **T. Mohsenin** and T. Oates, "Deep Belief Networks used on High Resolution Multichannel Electroencephalography Data for Seizure Detection" In Proceedings of The AAAI Spring Symposium, March 2014

W3. **T. Mohsenin** and T. Oates, "Algorithm and Hardware Characterization for Personalized Big Data Analysis: A Case study for Seizure Detection", The 2014 NIST Data Science Symposium, March 2014

W2. **Tinoosh Mohsenin**, Jordan Bisasky and Darin Chandler, "A Many-core Platform for Intelligent Biomedical Systems", In Proceedings of the Grace Hopper Celebration of Women in Computing 2012 New Investigators Technical Papers (GHC'12), **Invited young investigator speaker**, November 2012

W1. **Tinoosh Mohsenin**, "Implementing Low Power Error Correction Hardware for Next Generation Communication Applications," In Proceedings of the Grace Hopper Celebration of Women in Computing 2011 New Investigators Technical Papers (GHC'11), **Invited young investigator speaker**, November 2011

A3. Amey Kulkarni and **Tinoosh Mohsenin** "Parallel heterogeneous architectures for efficient OMP compressive sensing reconstruction", In proceedings of The SPIE Sensing Technology and Applications Conference, May 2014.

A2. Mahmood, T., Cannon, B., Astar, W., Boudra, P., **Mohsenin, T.**, Carter, G, "I Polarization-insensitive All-optical Data Transfer using Cross-Phase Modulation in a PCF", In Proceedings of The SPIE Photonics North Conference, May 2014

A1. Asmita Korde, Damon Bradley, **Tinoosh Mohsenin** "Detection Performance and Hardware Complexity Analysis of Radar Compressive Sensing", In proceedings of The SPIE Conference on Defense, Security, and Sensing, May 2013

Press Release and Coverage

N7. UMBC News Story
http://news.umbc.edu/tinoosh-mohsenin-receives-nearly-500000-nsf-career-award-for-deep-learning-technologies/

N6. CSEE News Story
https://www.csee.umbc.edu/2017/04/umbc-prof-tinoosh-mohsenin-receives-nsf-career-award-deep-learning-technologies/

N6. UMBC Magazine, "UMBC Researchers Explore the New Great Frontier – The Brain"
http://magazine.umbc.edu/staking-our-claim/

N5. Huffington Post Interview, To appear 2017

N4. UMBC Discovery Magazine, "THE BODY ELECTRIC"
http://umbcmagazine.wordpress.com/umbc-magazine-winter-2014/discovery-winter-2014/ , Winter 2014

N3. UMBC Front Webpage, "THE BODY ELECTRIC",
http://umbc.edu/window/body_electric_2013.html, Fall 2013

N2. California AGGIE, UC Davis, "New 167-processor chip boasts high speed, energy efficiency", http://asucd-cms.ucdavis.edu/aggie-clone/2009/04/29/new-167processor-chip-boasts-high-speed-energy-efficiency/, April 2009

N1. UC Davis News Service, "New 167-processor Chip Is Super-fast, Ultra Energy-efficient",
http://www.news.ucdavis.edu/search/news_detail.lasso?id=9082, April 2009

Selected Invited Talks

T34. Army Research lab (ARL), Aberdeen Proving Ground, MD, Seminar
"Brain EEG Artifact Removal and Smart Health Monitoring", August 2017

T33. University College London (UCL), London, UK, Seminar,
"Towards an Energy Efficient Internet of Things Processing Platform", June 2017

T32. COEIT CAREER Workshop, UMBC, Baltimore, MD
"Lessons from my CAREER", May 2017

T31. President's Council, UMBC, Baltimore, MD
"NSF CREER DeepMatter: A Scalable & Programmable Embedded Deep Neural Network", April 2017

T30. DARPA SAGA Workshop, Dayton, OH, Seminar
"Efficient Accelerator for Mont Carlo Markov Chain Computing", November 2016

T29. Intel Corporation, Portland, OR, Seminar
"Towards a Secured Cognitive Internet of Things Processing Platform", June 2016

T28. Department of Energy (DOE) Neuromorphic Computing Workshop, Oak ridge National Lab, TN, Seminar, "Bringing Physical Dimensions to the Deep Networks for Neuromorphic Computing", June 2016

T27. 49th IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, Invited session, “Sketching-based High-Performance Biomedical Big Data Processing Accelerator”, May 2016

T26. 49th IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, Canada, Invited session, “Wearable Seizure Detection using Convolutional Neural Networks with Transfer Learning”, May 2016

T25. Army Research lab (ARL), Aberdeen Proving Ground, MD, Seminar
“Algorithms, Architectures and Circuits for Personalized Smart Health Monitoring”, December 2015

T24. Telemedicine and Advanced Technology Research Center (TATRC)
“Low Power Signal Processing and Hardware for Smart Health Monitoring, June 2015

T23. University College London (UCL), London, UK, Seminar,
“Low Power Signal Processing and Hardware for Smart Health Monitoring, June 2015

T22. Naval Research lab (NRL), Washington DC, Seminar,
“Algorithms, Architectures and Circuits for Personalized Smart Health Monitoring”, June 2014

T21. Case Western Reserve University, Cleveland, OH, EECS Seminar
“Energy Efficient and High Performance Algorithms and Hardware for Biomedical Signal Processing and Communications Applications”, April 2014

T20. NASA Goddard, Greenbelt, MD, Digital Signal Processing Technology group Seminar
“Efficient Implementation of DSP and Communications Applications in Low Power Hardware”, March 2014

T19. Hughes Networks Systems LLC, Germantown, MD, Seminar,
“Energy Efficient and High Performance Architectures for Communication Applications”, September 2013

T18. Information Sciences Institute (ISI) , Arlington, VA, Seminar,
“Algorithms, Architectures and Circuits for Complex DSP and ML Applications ”, August 2013

T17. Imperial College, London, UK, EE Department, Research Group Seminar
“Algorithms, Architectures and Circuits for Complex DSP and ML Applications, July 2013

T16. IEEE Signal Processing Chapter, Baltimore, MD, Seminar
“Energy Efficient Platforms for High Performance and Embedded Computing”, May 2013

T15. Nokia Research Lab, Berkeley, CA, Seminar
“Energy Efficient Platforms for High Performance and Embedded Computing”, March 2013

T14. NASA Goddard, Digital Signal Processing Technology group Seminar
“Efficient Implementation of Compressive Sensing Reconstruction”, September 2012

T13. IEEE Circuits and Solid States, Baltimore, MD, Seminar
“Energy Efficient and High Performance Architectures for Communication Applications”, November 2011

T12. Telemedicine and Advanced Technology Research Center (TATRC), A Multi-channel Seizure Detection and Analysis Chip, September 2011

T12. University of California, San Diego, TATRC-Qualcomm Wireless Health Innovation Challenge Talk “Wireless Lab-on-a-Chip Apparatus, for Implantable Cardiac Devices”, February 2011

T11. Marvell Technology Group, Santa Clara, CA, Seminar
"Energy Efficient and High Performance Architectures for Communication Applications", April 2010.

T10. University of Washington, FPGA Seminar
"Algorithms and Architectures for Efficient Low Density Parity Check (LDPC) Decoder Hardware", December 2009.

T8.Rice University, ECE Seminar
"A 32 Gbps 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder Using Split-Row Threshold Decoding Method ", September 2009.

T7.Texas Instruments, Dallas, TX, Research Seminar
"A 1.6 W 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder", September 2009.

T6. IEEE Santa Clara Valley (SCV) Solid State Circuits Society, Santa Clara, CA, Seminar, "A 32 Gbps 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder Using Split-Row Threshold Decoding Method", August 2009.

T5. Aquantia, Milpitas, CA, Technical Meeting, "A 32 Gbps 2048-bit 10GBASE-T Ethernet Energy Efficient LDPC Decoder Using Split-Row Threshold Decoding Method", July 2009.

T4. National Chiao Tung University (NCTU), Taiwan, Research Group Seminar
"Efficient DSP Hardware Implementations", May 2009.

T3. National Taiwan University (NTU), Taiwan, Research Group Meeting, "Efficient DSP Hardware Implementations", May 2009.

T2. Plato Networks, Santa Clara, CA, Technical Meeting, "High Throughput and Low Power LDPC Decoders Using Split-Row Decoding Methods", February 2008.

T1. Jet Propulsion Laboratory (JPL) at the California Institute of Technology, Seminar "High Throughput and Low Power LDPC Decoders Using Split-Row Decoding Methods", March 2008.

Teaching

CMPE 311: Embedded Systems and C programming (Fall 2015, Fall 2016, Fall 2017)

CMPE 415 Programmable Logic Devices (Fall 2011, Spring 2012, Spring 2013, Spring 2014, Spring 2017), developed most of the material for the course

CMPE 691/491 Digital Signal Processing Hardware Implementation (Spring 2011, Spring 2012, Fall 2013, Fall 2014), developed a complete new course

CMPE 650 Digital Systems (Spring 2013, Spring 2014, Spring 2015, Spring 2016, Spring 2017), developed most of the material for the course

CMPE 641 Advanced Topics in VLSI (Spring 2016), co-taught and co-developed new material for the course

Service to the Department, University, Community, and Profession

Service to the Department

Committees

Undergraduate Committee, Member, Fall 2014- Present
CSEE Faculty Search Committee, Member, Fall 2015-May 2016
Department Chair Search Committee, Member, December 2015-Mar 2015
ECE Graduate Committee, Member, Spring 2011-Fall 2014
ECE Faculty Search Committee, Member, Fall 2014-May 2015
Department Executive Committee, Member, Spring 2013-Jue 2015
Northrop Grumman-UMBC Graduate Fellowship Committee, Member, Spring 2014-2015

Other

Academic adviser for 15 Undergraduate Computer Engineering Majors, Spring 2014-Present
Mentor for The Center for Women In Technology (CWIT) Scholars, Fall 2015- Present
Judge for Engineering Design Competitions for High School Girls, February 2012

Professional Service

Editorial Board

Associate Editor IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), 2016-2017
Associate Editor IEEE Transactions on Circuits and Systems-I (TCAS-I), 2015-2016

Conference Chair Activities

Local Arrangement Chair for the 50th IEEE International Symposium on Circuits and Systems (ISCAS'17) with over 1000 participants, Baltimore, May 2017. ISCAS is among most traditional conferences in Circuits and Systems. My responsibilities include two initiatives for the conference: 1. Student Travel Award for 26 US students through a $30K NSF grant submitted by me through UMBC 2. Child Care support through Helping Hand Inc.

Special Session Organizer/Session Chair

Session Organizer and Chair, "Deep Learning for Embedded Real Time Systems", 50th IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, US, May 2017

Session Organizer and Co-Chair, "Ultra-efficient Approaches Enabling Long-term, Mobile EEG for Brain Monitoring", 50th IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, US, May 2017

Session Organizer and Chair, "Wearable Biomedical Big Data Computing Session", 49th IEEE International Symposium on Circuits and Systems (ISCAS'16), Montreal, CA, May 2016

Session Chair, "Biomedical Signal Processing Track", IEEE International Symposium on Biomedical Circuits and Systems (BioCAS), Atlanta, Oct. 2015

Session Chair, "Brain Computer Interface and Processing Track", IEEE International Symposium on Biomedical Circuits and Systems (BioCAS'15), Atlanta, Oct. 2015

Session Chair, "Biomedical Signal Processing and Systems", 48th IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, May 2015

Session Chair, 24th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Washington DC, May 2013

Session Chair, 44th IEEE International Symposium on Circuits and Systems (ISCAS), Rio de Janeiro, Brazil, May 2011

Session Chair, 45th IEEE Conference on Information Sciences and Systems (CISS), Baltimore, March 2011

Secretary

IEEE P1890 Standard Committee for Error Correction Coding of Flash Memory, 2013- present

Technical Program Committee (TPC)

IEEE International Solid-State Circuits Conference-Student Research (ISSCC-SRP), 2013-present

IEEE Biomedical Circuits and Systems Conference (BioCAS), 2011-present

IEEE Women in Circuits and Systems Workshop (WiCAS), 2011-present

IEEE International Symposium on Quality Electronic Design (ISQED), 2012-2015

IEEE Life Science Systems and Applications Workshop (LiSSA), 2011-2012

Grant Proposal Panel Member and Reviewer

Six NSF Panels at the Directorate for Computer and Information Science (CISE): Two panels at Computing and Communication Foundations (CCF), one Panel in Software Hardware Foundation (SHF), two Panels in Secure and Trustworthy Cyberspace Program (SATc), and one Panel in Smart Health and Connected Program (SCH), 2011-2016.

Reviewer

IEEE Journal of Solid-State Circuits (JSSC)
IEEE Transactions on Circuits and Systems-I and II (TCAS-I, TCAS-II)
IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)
IEEE Transactions on Signal Processing (TSP)
IEEE Transaction on Biomedical Circuits and Systems (BioCAS)
IEEE Transactions on Neural Systems and Rehabilitation Engineering
IEEE International Symposium on Circuits and Systems (ISCAS)
IEEE International Conference on Computer Design (ICCD)
IEEE International Symposium on Quality Electronic Design (ISQED)
IEEE Biomedical Circuits and Systems (BioCAS)
IEEE International Solid-State Circuits Conference-Student Research (ISSCC-SRP)