EE-612: Lecture 22: CMOS Process Steps

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Fall 2006
outline

1) Unit Process Operations
2) Process Variations
unit process operations

1) Oxidation
2) Diffusion
3) Ion Implantation
4) RTA/RTP
5) Chemical Vapor Deposition
6) Lithography
7) Etching
8) Metalization
9) Well Structures
10) Isolation
11) Source / Drain structures
useful references


oxidation

\[ \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \text{ (dry)} \]
\[ \text{Si} + \text{H}_2\text{O} \rightarrow \text{SiO}_2 \text{ (wet)} \]

\[ T = 800 - 1100 \, ^\circ\text{C} \]

- fused quartz furnace tube
- heater
- wafers
oxidation and doping

\[ m = \frac{C_{Si}}{C_{SiO_2}} \]
local oxidation

$Si_3N_4$

$SiO_2$

$Si$
local oxidation (LOCOS)

'Si$_3$N$_4$'

'SiO$_2$'

'Si'

'field oxide'
constant source diffusion

\[ C(x) = C_s \text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \]

\[ Q = \int_0^\infty C(x,t) dx = 2C_s\sqrt{Dt/\pi} \]

dopant-containing gas (e.g. POCl\(_3\))

\(x\)

\(C\)

\(C_s\)
Limited source diffusion

\[ C(x,t) = \left( \frac{Q}{\sqrt{\pi Dt}} \right) \exp \left[ -\left( \frac{x}{2\sqrt{Dt}} \right)^2 \right] \]
diffusion

substitutional

interstitialcy

interstitial

\[ D(T) = D_0 e^{-E_A/k_B T} \]

“oxidation enhanced diffusion’
ion implantation

energetic ions bombard silicon wafer

\[ \vec{F} = Q \nu \times \vec{B} \]

ion source

magnet

acceleration

deflection

wafer
ion implantation

\[ N(x) = N_p \exp\left[ -\left( x - R_p \right)^2 / 2\Delta R_p^2 \right] \]

\[ Q = 2\pi N_p \Delta R_p \]

Implant damage (anneal)
ion implantation (ii)

![Graph showing the relationship between projected range (µm) and acceleration energy (keV) for different elements. B and As are marked on the graph.](image)
channeling

\[ C(x) \]

\[ \Delta R_P \]

tilted 3 deg
rapid thermal annealing

reflector

lamps

quartz window

wafer

gas inlet

thermal budget

$\sqrt{Dt}$
chemical vapor deposition

reaction chamber

\[ \sqrt{Dt} \]

gas inlet

\[ \text{wafer} \]

\[ \text{susceptor} \]

gas exhaust

\[ 2\text{SiH}_4 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 12\text{H}_2 \]  
  silicon nitride

\[ \text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2 \]  
  poly silicon

\[ \text{SiH}_4 + \text{O}_2 \rightarrow \text{SiO}_2 + 2\text{H}_2 \]  
  silicon dioxide
plasma CVD / etching

lower temperature reduces thermal budget $\sqrt{Dt}$
lithography

- optical source
- wavelength, $\lambda$
- lens
- shutter
- mask
- resist
- wafer

expose, develop, etch
projection printing

UV source

lens 1

mask

lens 2

wafer

\[ \alpha \]
registration errors

misalignment    run out
phase shift lithography

conventional mask

phase shift mask

electric field at mask

electric field at mask

intensity at wafer

intensity at wafer
pattern transfer

resist:
optically sensitive polymer which, when exposed to UV changes its solubility in specific chemicals

negative resist
(less soluble after exposure)

positive resist
(more soluble after exposure)
etching

wet chemical etching
(isotropic)

chemicals react with
underlying material,
but not resist

undercut

dry etching (plasma or reactive ion
etching - RIE)
(anisotropic)

ionized gases react
with underlying
material, but not resist
pattern transfer (ii)

mask

$L_{\text{Drawn}}$

chrome

lithography bias

etch bias

resist

$L_{\text{Gate}}$ (physical)
10 Interconnect

Tungsten (W) plugs for first layer metal dep CMP

Figure 70  Cross-section of Hierarchical Scaling—MPU Device
outline

1) Unit Process Operations
2) Process Variations
discrete doping effects

Number of dopants in the critical volume is a **statistical quantity**

\[ V = W \times L \times x_j \]

example:
\[
\begin{align*}
L &= 50 \text{ nm} \\
W &= 100 \text{ nm} \\
x_j &= 25 \text{ nm} \\
N_A &= 10^{18} \text{ cm}^{-3} \\
N_{TOT} &= 125
\end{align*}
\]
discrete doping effects (ii)

3D transport leads to inhomogeneous conduction

Effects:

1) $\sigma_{V_T}$ (10’s of mV)
2) lower avg. $V_T$ (10’s of mV)
3) asymmetry in $I_D$

(see Wong and Taur, IEDM, 1993, p. 705)
discrete doping effects (iii)

AFM measurements, Fujitsu

(simulations from A. Asenov group, Univ. of Glasgow)
statistical variability

Line edge roughness

discrete dopants

The simulation Paradigm now

A 22 nm MOSFET In production 2008

From A. Asenov, Univ. of Glasgow
variability is becoming a major issue

G. Declerck, Keynote talk, VLSI Technol. Symp. 2005
1) Unit Process Operations
2) Process Variations

For a basic, CMOS process flow for an STI (shallow trench isolation process), see:
CMOS process flow

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The author is indebted to Dr. Lynn Fuller of Rochester Institute of Technology for making these materials available. What follows is a condensed version of a more complete presentation by Dr. Fuller. I regret any errors that I may have introduced by shortening these materials. -Mark Lundstrom 10/19/06