CMSC 611: Advanced Computer Architecture

Pipelining
Washer takes 30 min, Dryer takes 40 min, folding takes 20 min

Sequential laundry takes 6 hours for 4 loads

If they learned pipelining, how long would laundry take?
- Pipelining means start work as soon as possible
- Pipelined laundry takes 3.5 hours for 4 loads
Pipelining doesn’t help latency of single task, it helps throughput of entire workload.

Pipeline rate limited by slowest pipeline stage.

Multiple tasks operating simultaneously using different resources.

Potential speedup = Number pipe stages.

Unbalanced lengths of pipe stages reduces speedup.

Time to “fill” pipeline and time to “drain” it reduce speedup.

Stall for Dependencies.
**MIPS Instruction Set**

- RISC characterized by the following features that simplify implementation:
  - All ALU operations apply only on registers
  - Memory is affected only by load and store
  - Instructions follow very few formats and typically are of the same size

<table>
<thead>
<tr>
<th>Bit</th>
<th>Operation (op)</th>
<th>Register (rs)</th>
<th>Register (rt)</th>
<th>Register (rd)</th>
<th>Shift (shamt)</th>
<th>Function (funct)</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-26</td>
<td>6 bits</td>
<td>5 bits</td>
<td>5 bits</td>
<td>5 bits</td>
<td>5 bits</td>
<td>6 bits</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Operation (op)</th>
<th>Register (rs)</th>
<th>Register (rt)</th>
<th>Immediate</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-26</td>
<td>6 bits</td>
<td>5 bits</td>
<td>5 bits</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Operation (op)</th>
<th>Target Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-26</td>
<td>6 bits</td>
<td>26 bits</td>
</tr>
</tbody>
</table>
Single-cycle Execution
Multi-Cycle Implementation of MIPS

1. Instruction fetch cycle (IF)
   \[ IR \leftarrow \text{Mem}[PC]; \quad NPC \leftarrow PC + 4 \]

2. Instruction decode/register fetch cycle (ID)
   \[ A \leftarrow \text{Regs}[IR_{6..10}]; \quad B \leftarrow \text{Regs}[IR_{11..15}]; \quad \text{Imm} \leftarrow ((IR_{16})^{16} ## IR_{16..31}) \]

3. Execution/effective address cycle (EX)
   Memory ref: \[ \text{ALUOutput} \leftarrow A + \text{Imm}; \]
   Reg-Reg ALU: \[ \text{ALUOutput} \leftarrow A \text{ func } B; \]
   Reg-Imm ALU: \[ \text{ALUOutput} \leftarrow A \text{ op } \text{Imm}; \]
   Branch: \[ \text{ALUOutput} \leftarrow NPC + \text{Imm}; \quad \text{Cond} \leftarrow (A \text{ op } 0) \]

4. Memory access/branch completion cycle (MEM)
   Memory ref: \[ \text{LMD} \leftarrow \text{Mem} \left[ \text{ALUOutput} \right] \quad \text{or} \quad \text{Mem} \left[ \text{ALUOutput} \right] \leftarrow B; \]
   Branch: \[ \text{if (cond) PC} \leftarrow \text{ALUOutput}; \]

5. Write-back cycle (WB)
   Reg-Reg ALU: \[ \text{Regs}[IR_{16..20}] \leftarrow \text{ALUOutput}; \]
   Reg-Imm ALU: \[ \text{Regs}[IR_{11..15}] \leftarrow \text{ALUOutput}; \]
   Load: \[ \text{Regs}[IR_{11..15}] \leftarrow \text{LMD}; \]
Multi-cycle Execution

Figure: Dave Patterson
The load instruction is the longest

All instructions follow at most the following five steps:

- **Ifetch**: Instruction Fetch
  - Fetch the instruction from the Instruction Memory and update PC
- **Reg/Dec**: Registers Fetch and Instruction Decode
- **Exec**: Calculate the memory address
- **Mem**: Read the data from the Data Memory
- **WB**: Write the data back to the register file
Pipelining improves performance by increasing instruction throughput.

Program Flow

- Start handling next instruction while the current instruction is in progress
- Feasible when different devices at different stages

\[
\text{Time between instructions}_{\text{pipelined}} = \frac{\text{Time between instructions}_{\text{nonpipelined}}}{\text{Number of pipe stages}}
\]
Ideal and upper bound for speedup is number of stages in the pipeline.

Example of Instruction Pipelining

Program execution order (in instructions)

1. lw $1, 100($0)
2. lw $2, 200($0)
3. lw $3, 300($0)

Time

2 4 6 8 10 12 14 16 18

Instruction fetch | Reg | ALU | Data access | Reg

Instruction fetch | Reg | ALU | Data access | Reg

Time between first & fourth instructions is $3 \times 8 = 24$ ns

Program execution order (in instructions)

1. lw $1, 100($0)
2. lw $2, 200($0)
3. lw $3, 300($0)

Time

2 4 6 8 10 12 14

Instruction fetch | Reg | ALU | Data access | Reg

Instruction fetch | Reg | ALU | Data access | Reg

Time between first & fourth instructions is $3 \times 2 = 6$ ns

Ideal and upper bound for speedup is number of stages in the pipeline.
• Cycle time long enough for longest instruction
• Shorter instructions waste time
• No overlap
- Cycle time long enough for longest stage
- Shorter stages waste time
- Shorter instructions can take fewer cycles
- No overlap
- Cycle time long enough for longest stage
- Shorter stages waste time
- No additional benefit from shorter instructions
- Overlap instruction execution
Pipeline Performance

• Pipeline increases the instruction throughput
  – not execution time of an individual instruction
• An individual instruction can be slower:
  – Additional pipeline control
  – Imbalance among pipeline stages
• Suppose we execute 100 instructions:
  – Single Cycle Machine
    • 45 ns/cycle x 1 CPI x 100 inst = 4500 ns
  – Multi-cycle Machine
    • 10 ns/cycle x 4.2 CPI (due to inst mix) x 100 inst = 4200 ns
  – Ideal 5 stages pipelined machine
    • 10 ns/cycle x (1 CPI x 100 inst + 4 cycle drain) = 1040 ns
• Lose performance due to fill and drain
Pipeline Datapath

- Every stage must be completed in one clock cycle to avoid stalls.
- Values must be latched to ensure correct execution of instructions.
- The PC multiplexer has moved to the IF stage to prevent two instructions from updating the PC simultaneously (in case of branch instruction).
### Pipeline Stage Interface

<table>
<thead>
<tr>
<th>Stage</th>
<th>Any Instruction</th>
</tr>
</thead>
</table>
| **IF** | IF/ID.IR \(\leftrightarrow\) MEM[PC] ;  
IF/ID.NPC,PC \(\leftarrow\) ( if ( (EX/MEM.opcode == branch) & EX/MEM.cond) 
{EX/MEM.ALUOutput } else { PC + 4 } ) ;  
ID/EX.NPC \(\leftarrow\) IF/ID.NPC ; ID/EX.IR \(\leftarrow\) IF/ID.IR;  
ID/EX.Imm \(\leftarrow\) (IF/ID. IR \(_{16}\) \^{16} ## IF/ID. IR \(_{16..31}\); |
| **ID** | ID/EX.A = Regs[IF/ID. IR \(_{6..10}\)]; ID/EX.B \(\leftarrow\) Regs[IF/ID. IR \(_{11..15}\)];  
ID/EX.NPC \(\leftarrow\) IF/ID.NPC ; ID/EX.IR \(\leftarrow\) IF/ID.IR;  
ID/EX.Imm \(\leftarrow\) (IF/ID. IR \(_{16}\) \^{16} ## IF/ID. IR \(_{16..31}\); |
<table>
<thead>
<tr>
<th><strong>EX</strong></th>
<th>ALU</th>
<th>Load or Store</th>
<th>Branch</th>
</tr>
</thead>
</table>
| EX/MEM.IR \(\leftarrow\) ID/EX.IR;  
EX/MEM.ALUOutput \(\leftarrow\) ID/EX.A func ID/EX.B;  
Or  
EX/MEM.ALUOutput \(\leftarrow\) ID/EX.A op ID/EX.Imm;  
EX/MEM.cond \(\leftarrow\) 0; | EX/MEM.IR \(\leftarrow\) ID/EX.IR;  
EX/MEM.ALUOutput \(\leftarrow\) ID/EX.A + ID/EX.Imm;  
EX/MEM.cond \(\leftarrow\) 0;  
EX/MEM.B \(\leftarrow\) ID/EX.B; | EX/MEM.ALUOutput \(\leftarrow\) ID/EX.NPC + ID/EX.Imm;  
EX/MEM.cond \(\leftarrow\) (ID/EX.A op 0); |
| MEM/WB.IR \(\leftarrow\) EX/MEM.IR;  
MEM/WB.ALUOutput \(\leftarrow\) EX/MEM.ALUOutput; | MEM/WB.IR \(\leftarrow\) EX/MEM.IR;  
MEM/WB.LMD \(\leftarrow\) Mem[EX/MEM.ALUOutput] ;  
Or  
Mem[EX/MEM.ALUOutput] \(\leftarrow\) EX/MEM.B ; |  |
| WB | Regs[MEM/WB. IR \(_{16..20}\}] \(\leftarrow\) EM/WB.ALUOutput;  
Or  
Regs[MEM/WB. IR \(_{11..15}\}] \(\leftarrow\) MEM/WB.ALUOutput ; | For load only:  
Regs[MEM/WB. IR \(_{11..15}\}] \(\leftarrow\) MEM/WB.LMD; |  |
Pipeline Hazards

- Cases that affect instruction execution semantics and thus need to be detected and corrected

- Hazards types
  - **Structural hazard**: attempt to use a resource two different ways at same time
    - Single memory for instruction and data
  - **Data hazard**: attempt to use item before it is ready
    - Instruction depends on result of prior instruction still in the pipeline
  - **Control hazard**: attempt to make a decision before condition is evaluated
    - branch instructions

- Hazards can always be resolved by waiting
Example: One Memory Port/Structural Hazard

Time (clock cycles)

Cycle 1 | Cycle 2 | Cycle 3 | Cycle 4 | Cycle 5 | Cycle 6 | Cycle 7

Load

Instr 1

Instr 2

Instr 3

Instr 4

Structural Hazard

Slide: David Culler
1. Wait
   - Must detect the hazard
     • Easier with uniform ISA
   - Must have mechanism to stall
     • Easier with uniform pipeline organization
2. Throw more hardware at the problem
   - Use instruction & data cache rather than direct access to memory
Detecting and Resolving Structural Hazard

Time (clock cycles)

Cycle 1 | Cycle 2 | Cycle 3 | Cycle 4 | Cycle 5 | Cycle 6 | Cycle 7
--- | --- | --- | --- | --- | --- | ---
Load | Ifetch | Reg | ALU | DMem | Reg | Ifetch | Reg
Instr 1 | Reg | ALU | DMem | Reg | Ifetch | Reg
Instr 2 | Reg | ALU | DMem | Reg
Stall | | Bubble | Bubble | Bubble | Bubble | Bubble
Instr 3 | Ifetch | Reg | ALU | DMem | Reg | Ifetch | Reg

Slide: David Culler
Stalls & Pipeline Performance

Pipelining Speedup = \frac{\text{Average instruction time unpipelined}}{\text{Average instruction time pipelined}}

= \frac{\text{CPI unpipelined}}{\text{CPI pipelined}} \times \frac{\text{Clock cycle unpipelined}}{\text{Clock cycle pipelined}}

Ideal CPI pipelined = 1

CPI pipelined = \text{Ideal CPI} + \text{Pipeline stall cycles per instruction}

= 1 + \text{Pipeline stall cycles per instruction}

Speedup = \frac{\text{CPI unpipelined}}{1 + \text{Pipeline stall cycles per instruction}} \times \frac{\text{Clock cycle unpipelined}}{\text{Clock cycle pipelined}}

Assuming all pipeline stages are balanced

Speedup = \frac{\text{Pipeline depth}}{1 + \text{Pipeline stall cycles per instruction}}
Data Hazards

Time (clock cycles)

Instr. Order

add \( r_1, r_2, r_3 \)

sub \( r_4, r_1, r_3 \)

and \( r_6, r_1, r_7 \)

or \( r_8, r_1, r_9 \)

xor \( r_{10}, r_1, r_{11} \)

Slide: David Culler
Three Generic Data Hazards

• Read After Write (RAW)
  Instr\textsubscript{J} tries to read operand before Instr\textsubscript{I} writes it

\[ 
\begin{align*}
\text{I: } & \text{ add } r1, r2, r3 \\
\text{J: } & \text{ sub } r4, r1, r3 \\
\end{align*}
\]

• Caused by a “Data Dependence” (in compiler nomenclature). This hazard results from an actual need for communication.
Three Generic Data Hazards

• **Write After Read (WAR)**
  Instr\textsubscript{J} writes operand before Instr\textsubscript{I} reads it

  \[ I: \text{sub } r4, r1, r3 \]
  \[ J: \text{add } r1, r2, r3 \]
  \[ K: \text{mul } r6, r1, r7 \]

• Called an “anti-dependence” in compilers.
  – This results from reuse of the name “r1”.

• Can’t happen in MIPS 5 stage pipeline because:
  – All instructions take 5 stages, and
  – Reads are always in stage 2, and
  – Writes are always in stage 5
Three Generic Data Hazards

• **Write After Write (WAW)**
  Instr\textsubscript{J} writes operand before Instr\textsubscript{I} writes it.

  \[\text{I: } \text{mul } r1, r4, r3\]
  \[\text{J: } \text{add } r1, r2, r3\]
  \[\text{K: } \text{sub } r6, r1, r7\]

• Called an “output dependence” in compilers
  – This also results from the reuse of name “r1”.

• Can’t happen in MIPS 5 stage pipeline:
  – All instructions take 5 stages, and
  – Writes are always in stage 5

• Do see WAR and WAW in more complicated pipes
Forwarding to Avoid Data Hazard

Time (clock cycles)

Instruction Order

add r1, r2, r3

sub r4, r1, r3

and r6, r1, r7

or r8, r1, r9

xor r10, r1, r11
HW Change for Forwarding

NextPC

Registers

Immediate

ID/EX

mux

mux

mux

ALU

EX/MEM

Data Memory

MEM/WR

mux

Slide: David Culler
Data Hazard Even with Forwarding

\[ \text{lw } r1, 0(r2) \]
\[ \text{sub } r4, r1, r6 \]
\[ \text{and } r6, r1, r7 \]
\[ \text{or } r8, r1, r9 \]
Resolving Load Hazards

- Adding hardware? How? Where?
- Detection?
- Compilation techniques?
- What is the cost of load delays?
Resolution of the Load Data Hazard

**lw r1, 0(r2)**

**sub r4, r1, r6**

**and r6, r1, r7**

**or r8, r1, r9**

How is this different from the instruction issue stall?
Try producing fast code for

\[ a = b + c; \]
\[ d = e - f; \]

assuming \( a, b, c, d, e, \) and \( f \) in memory.

<table>
<thead>
<tr>
<th>Slow code</th>
<th>Fast code</th>
</tr>
</thead>
<tbody>
<tr>
<td>LW ( \text{Rb},b )</td>
<td>LW ( \text{Rb},b )</td>
</tr>
<tr>
<td>LW ( \text{Rc},c )</td>
<td>LW ( \text{Rc},c )</td>
</tr>
<tr>
<td>ADD ( \text{Ra,Rb},\text{Rc} )</td>
<td>ADD ( \text{Ra,Rb},\text{Rc} )</td>
</tr>
<tr>
<td>SW ( a,\text{Ra} )</td>
<td>LW ( \text{Rf},f )</td>
</tr>
<tr>
<td>LW ( \text{Re},e )</td>
<td>SW ( a,\text{Ra} )</td>
</tr>
<tr>
<td>LW ( \text{Re},e )</td>
<td>SUB ( \text{Rd},\text{Re},\text{Rf} )</td>
</tr>
<tr>
<td>LW ( \text{Rf},f )</td>
<td>SW ( d,\text{Rd} )</td>
</tr>
<tr>
<td>SUB ( \text{Rd},\text{Re},\text{Rf} )</td>
<td></td>
</tr>
<tr>
<td>SW ( d,\text{Rd} )</td>
<td></td>
</tr>
</tbody>
</table>
Instruction Set Connection

- What is exposed about this organizational hazard in the instruction set?
- k cycle delay?
  - bad, CPI is not part of ISA
- k instruction slot delay
  - load should not be followed by use of the value in the next k instructions
- Nothing, but code can reduce run-time delays
- MIPS did the transformation in the assembler
Cases that affect instruction execution semantics and thus need to be detected and corrected.

Hazards types

- **Structural hazard**: attempt to use a resource two different ways at same time
  - Single memory for instruction and data
- **Data hazard**: attempt to use item before it is ready
  - Instruction depends on result of prior instruction still in the pipeline
- **Control hazard**: attempt to make a decision before condition is evaluated
  - branch instructions

Hazards can always be resolved by waiting.
Control Hazard on Branches
Three Stage Stall

10: beq r1, r3, 36
14: and r2, r3, r5
18: or r6, r1, r7
22: add r8, r1, r9
36: xor r10, r1, r11
Example: Branch Stall Impact

- If 30% branch, 3-cycle stall significant!
- Two part solution:
  - Determine branch taken or not sooner, AND
  - Compute taken branch address earlier
- MIPS branch tests if register = 0 or ≠ 0
- MIPS Solution:
  - Move Zero test to ID/RF stage
  - Adder to calculate new PC in ID/RF stage
  - 1 clock cycle penalty for branch versus 3
Pipelined MIPS Datapath

Figure: Dave Patterson
Four Branch Hazard Alternatives

1. Stall until branch direction is clear
2. Predict Branch Not Taken
   - Execute successor instructions in sequence
   - “Squash” instructions in pipeline if branch taken
   - Advantage of late pipeline state update
   - 47% MIPS branches not taken on average
   - PC+4 already calculated, so use it to get next instruction
3. Predict Branch Taken
   - 53% MIPS branches taken on average
   - But haven’t calculated branch target address in MIPS
     • MIPS still incurs 1 cycle branch penalty
     • Other machines: branch target known before outcome
Four Branch Hazard Alternatives

4. Delayed Branch
   - Define branch to take place AFTER a following instruction
     branch instruction
     sequential successor$_1$
     sequential successor$_2$
     ........
     sequential successor$_n$

     Branch delay of length $n$

     branch target if taken

   - 1 slot delay allows proper decision and branch target address in 5 stage pipeline
   - MIPS uses this
Delayed Branch

• Where to get branch delay slot instructions?
  – Before branch instruction
  – From the target address
    • only valuable when branch taken
  – From fall through
    • only valuable when branch not taken
  – Canceling branches allow more slots to be filled

• Compiler effectiveness for single delay slot:
  – Fills about 60% of branch delay slots
  – About 80% of instructions executed in branch delay slots useful in computation
    – 48% (60% x 80%) of slots usefully filled

• Delayed Branch downside: 7-8 stage pipelines, multiple instructions issued per clock (superscalar)
Scheduling Branch-Delay Slots

Best scenario

ADD R1, R2, R3
if R2 = 0 then

Delay slot

Becomes

if R2 = 0 then
ADD R1, R2, R3

Good for loops

SUB R4, R5, R6
ADD R1, R2, R3
if R1 = 0 then

Delay slot

Becomes

ADD R1, R2, R3
if R1 = 0 then

SUB R4, R5, R6

Good taken strategy

ADD R1, R2, R3
if R1 = 0 then

SUB R4, R5, R6

R4 must be temp reg.
### Branch-Delay Scheduling Requirements

<table>
<thead>
<tr>
<th>Scheduling Strategy</th>
<th>Requirements</th>
<th>Improves performance when?</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) From before</td>
<td>Branch must not depend on the rescheduled instructions</td>
<td>Always</td>
</tr>
<tr>
<td>(b) From target</td>
<td>Must be OK to execute rescheduled instructions if branch is not taken. May need to duplicate instructions.</td>
<td>When branch is taken. May enlarge programs if instructions are duplicated.</td>
</tr>
<tr>
<td>(c) From fall through</td>
<td>Must be okay to execute instructions if branch is taken.</td>
<td>When branch is not taken.</td>
</tr>
</tbody>
</table>

- Limitation on delayed-branch scheduling arise from:
  - Restrictions on instructions scheduled into the delay slots
  - Ability to predict at compile-time whether a branch is likely to be taken
- May have to fill with a no-op instruction
  - Average 30% wasted
- Additional PC is needed to allow safe operation in case of interrupts (more on this later)
**Example: Evaluating Branch Alternatives**

Pipeline speedup = \( \frac{\text{Pipeline depth}}{1 + \text{Pipeline stall CPI}} \)

= \( \frac{\text{Pipeline depth}}{1 + \text{Branch frequency} \times \text{Branch penalty}} \)

Assume:

- 14% Conditional & Unconditional
- 65% Taken; 52% Delay slots not usefully filled

<table>
<thead>
<tr>
<th>Scheduling Scheme</th>
<th>Branch Penalty</th>
<th>CPI</th>
<th>Pipeline Speedup</th>
<th>Speedup vs stall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stall pipeline</td>
<td>3.00</td>
<td>1.42</td>
<td>3.52</td>
<td>1.00</td>
</tr>
<tr>
<td>Predict taken</td>
<td>1.00</td>
<td>1.14</td>
<td>4.39</td>
<td>1.25</td>
</tr>
<tr>
<td>Predict not taken</td>
<td>1.00</td>
<td>1.09</td>
<td>4.58</td>
<td>1.30</td>
</tr>
<tr>
<td>Delayed branch</td>
<td>0.52</td>
<td>1.07</td>
<td>4.66</td>
<td>1.32</td>
</tr>
</tbody>
</table>
Static Branch Prediction

- Examination of program behavior
  - Assume branch is usually taken based on statistics but misprediction rate still 9%-59%
- Predict on branch direction forward/backward based on statistics and code generation convention
  - Profile information from earlier program runs

![Bar chart showing instructions between misprediction for different benchmarks.](chart.png)