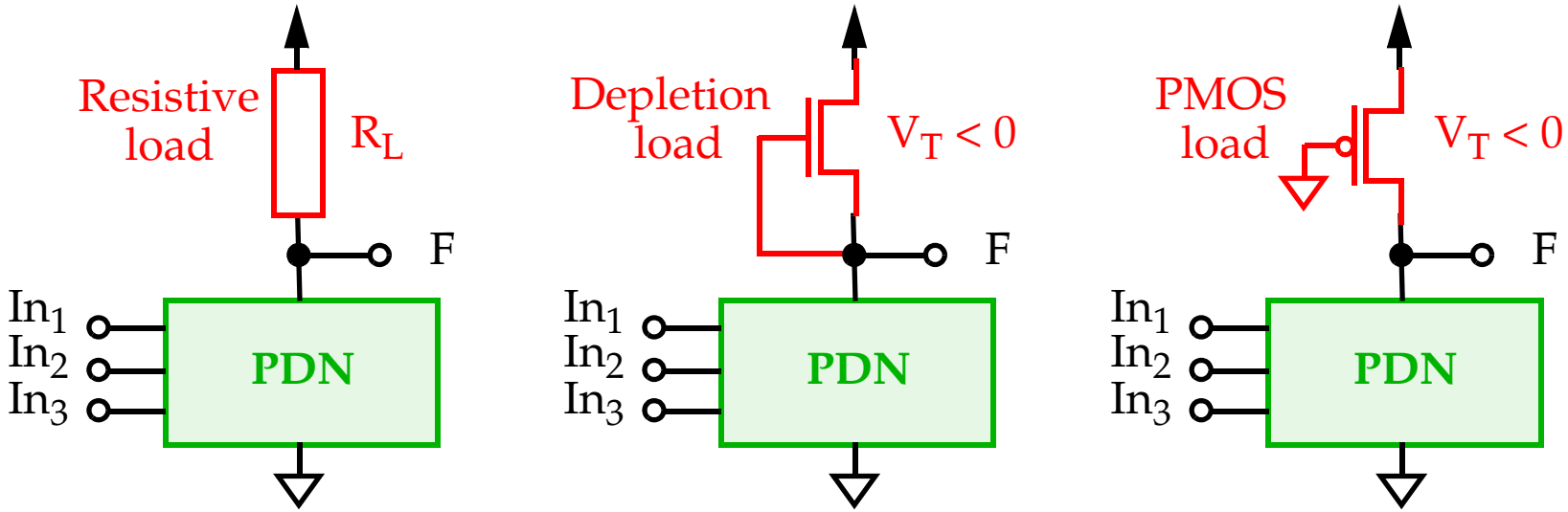
Ratioed Logic

One method to reduce the circuit complexity of static CMOS.

Here, the logic function is built in the PDN and used in combination with a simple load device.



Let's assume the load can be represented as **linearized resistors**.

When the PDN is on, the output voltage is determined by:

$$V_{OL} = \frac{R_{PDN}}{R_L + R_{PDN}} V_{DD}$$

Ratioed Logic

This logic style is called **ratioed** because care must be taken in scaling the impedances properly.

Note that full complementary CMOS is **ratioless**, since the output signals do not depend on the size of the transistors.

In order to keep the noise margins high, $R_L >> R_{PDN}$.

However, R_L must be able to provide as much current as possible to minimize delay.

$$t_{pLH} = 0.69 R_L C_L$$

$$t_{pHL} = 0.69 (R_L /\!/ R_{PDN}) C_L$$

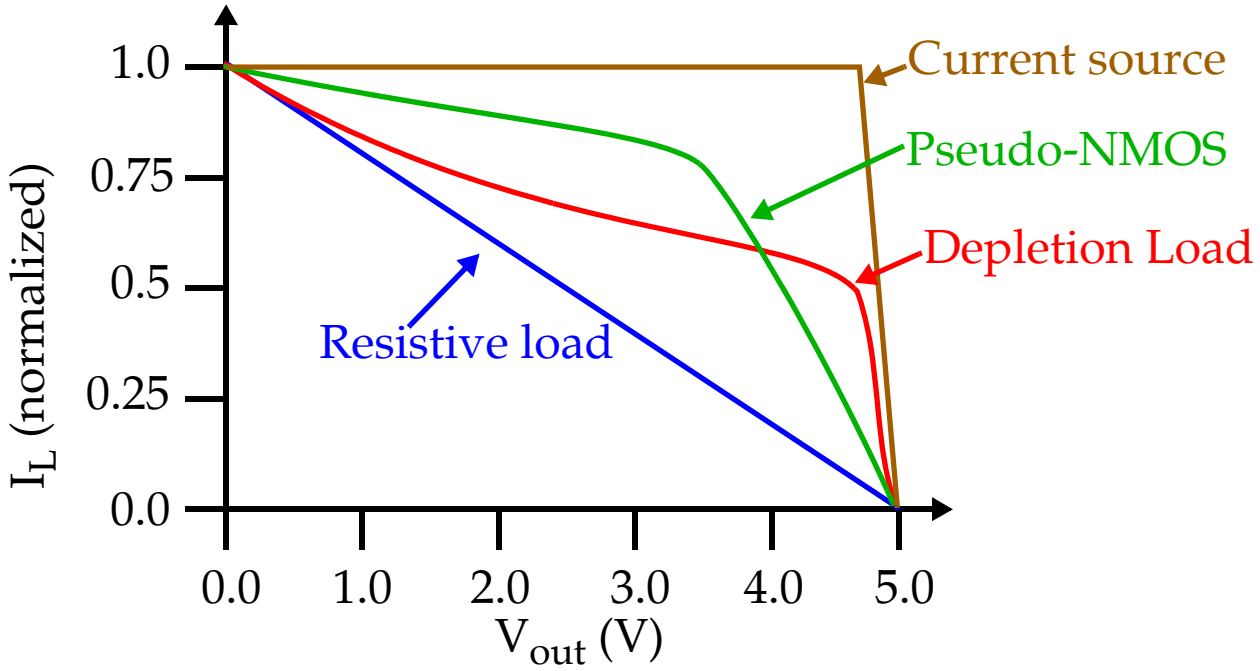
These are **conflicting** requirements:

R_L large: Noise margins.

R_L small: performance and power dissipation.

Ratioed Logic

This has resulted in a wide variety of possible load configurations.



- Simple resistor

  Available charge current as a function of the output voltage is linear:

$$I_L = \frac{V_{DD} - V_{out}}{R_L}$$

  Disadv: Charge current drops rapidly once V_{out} starts to rise.

Ratioed Logic

- Current source

  Ideal in the sense that the available current is independent of the output voltage.

  It is easy to prove that t_{pLH} is reduced by 25% over the resistor load.

- Depletion load

  The depletion load gate shown previously emerged as the *most popular* gate in the NMOS era (up until the early 80s).

  The load is an NMOS depletion mode transistor (*negative threshold device*) with the gate connected to the output (source).

  Note that the device is on when $V_{GS} = 0$.

  The load acts as a **current source** (first-order), given by its saturation equation:

$$I_L = \frac{k_{n,load}}{2}(|V_{Tn}|)^2$$

Ratioed Logic

- Depletion load (cont.)

  The load line *deviates* from the ideal current source for two reasons:

  (a) The **channel length modulation** factor modulates current in saturation mode.

  (b) The source of the load transistor is connected to the output of the inverter.

  The **body effect** causes the threshold of the load transistor to vary as a function of V_{out}.

  The body effect reduces $|V_{Tn}|$ and the available current for increasing values of V_{out}.

Nevertheless, the depletion load out-performs the resistive load and requires less area!

Ratioed Logic

- Pseudo-NMOS

A **grounded PMOS** device presents an even better load.

It is better than depletion NMOS because there is *no body effect* (its V_{SB} is constant and equal to 0).

Also, the PMOS device is driven by a $V_{GS} = -V_{DD}$, resulting in a higher load-current level than a similarly sized depletion-NMOS device.

$$I_L = \frac{k_p}{2}(V_{DD} - |V_{Tp}|)^2$$

(ignoring channel length modulation)

The V_{OH} ($=V_{DD}$) from the dc transfer characteristic is the same as that for the full complementary device.

V_{OL} differs from GND, however.

Ratioed Logic

- Pseudo-NMOS (cont)

  V_{OL} can be obtained by equating the currents through the driver and load devices for $V_{in} = V_{DD}$.

  Here, the **NMOS** driver resides in **linear mode** while the **PMOS** load is in **saturation**:

$$k_n\left((V_{DD} - V_{Tn})V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{k_p}{2}(V_{DD} - |V_{Tp}|)^2$$

  Assuming $V_{Tn} = |V_{Tp}|$, solving for V_{OL} yields:

$$V_{OL} = (V_{DD} - V_T)\left(1 - \sqrt{1 - \frac{k_p}{k_n}}\right)$$

  For example, if $k_p = k_n$, $V_{OL} = V_{DD} - V_T$, which is clearly unacceptable.

  For $r = k_p/k_n = 1/4$, $V_{OL} = (5 - 0.8)*0.134 \sim= 0.56V$.

Ratioed Logic

- Pseudo-NMOS (cont)

  Similarly, V_M can be computed by setting $V_{in} = V_{out}$ and solving the current equations

  This assumes the NMOS and PMOS are in **saturation** and **linear**, respectively.

$$V_M = V_T + (V_{DD} - V_T)\sqrt{\frac{k_p}{k_n + k_p}}$$

Design challenges:

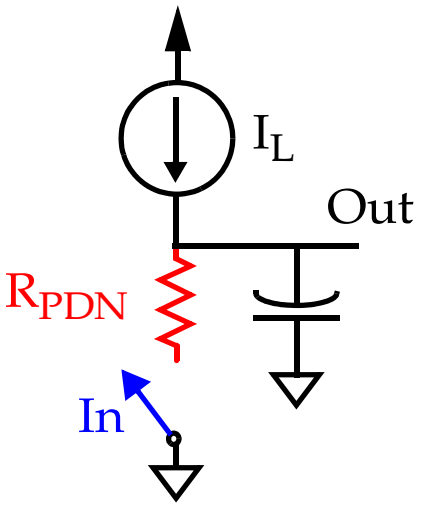
- This clearly indicates that V_M is **not** located in the middle of the voltage swing (e.g. if they are equal, the square root yields 0.707).
- The rise and fall times are **asymmetrical**.
- This gate consumes **static power** when the output is low.

$$P_{av} = V_{DD} I_{low} = \frac{k_p}{2} V_{DD} (V_{DD} - V_T)^2$$

Ratioed Logic

- Pseudo-NMOS (cont)

  Let's assume the load can be approximated as a *current source* for the entire operation region.



Trade-offs:

- To reduce static power, I_L **should be low**.
- To obtain a reasonable NM_L, $V_{OL} = I_L R_{PDN}$ **should be low**.
- To reduce $t_{pLH} \sim= (C_L V_{DD})/(2I_L)$, I_L **should be high**.
- To reduce $t_{pHL} \sim= 0.69 R_{PDN} C_L$, R_{PDN} should be kept **small**.

Ratioed Logic

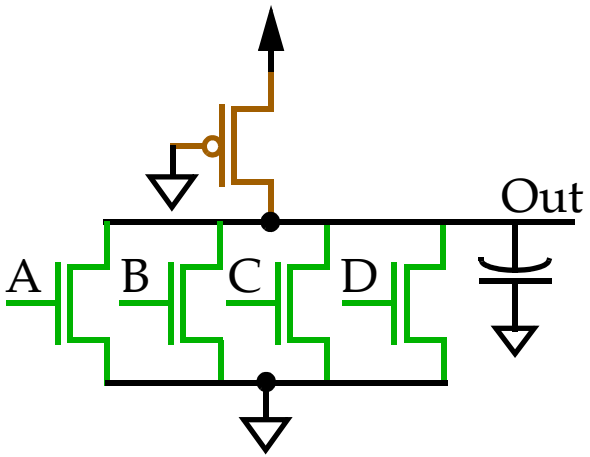
- Pseudo-NMOS (cont)

The r $= (W/L)_n/(W/L)_p$ in the expression for V_{OL} defines NM_L.

For example, to obtain a V_{OL} of 0.2V (1.2 um tech., V_{DD}=5V) requires a ratio of r=3. This also guarantees the 4th condition.

However, 1 and 3 **are contradictory**: realizing a faster gate (t_{pLH}) means more static power consumption and reduced noise margin.

Pseudo-NMOS attractive for complex gates with large fan-in.



As mentioned, only N+1 transistors, smaller area and smaller parasitics.

Smaller downstream load capacitance.

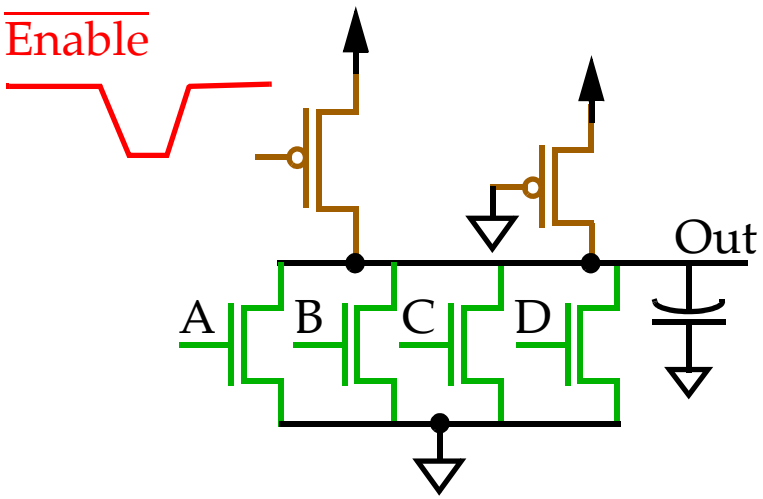
However, static power consumption makes it impossible to use in large circuits (except in address decoders when majority of outputs are high).

A minimum sized gate consumes 1mW !

Ratioed Logic

- Even better loads

  Consider the following modification to the pseudo-NMOS NOR.



Here, it is known that the inputs switch only during certain time periods.

For example, an address decoder which should only switch when the address changes.

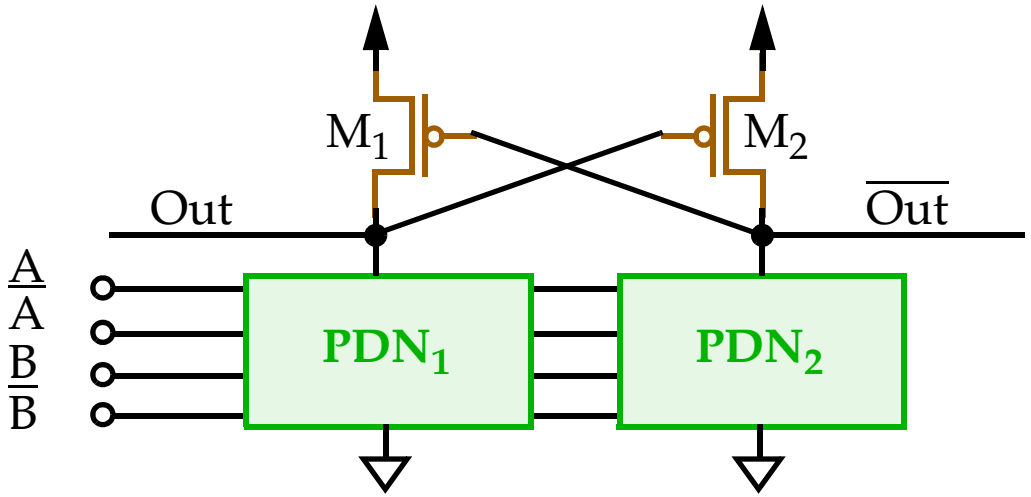
In stand-by mode, low power consumption and large noise margins.

For address change, high power fast t_{pLH} transition.

Ratioed Logic

- Even better loads (cont)

It's possible to **completely eliminate** static current:



Assumes signal and its complement are available

Differential Cascade Voltage Switch Logic (DCVSL).

PDN_1 and PDN_2 are complementary.

Assume PDN_1 conducts, input to M_2 is turned on, pulling up $\overline{Out}$.

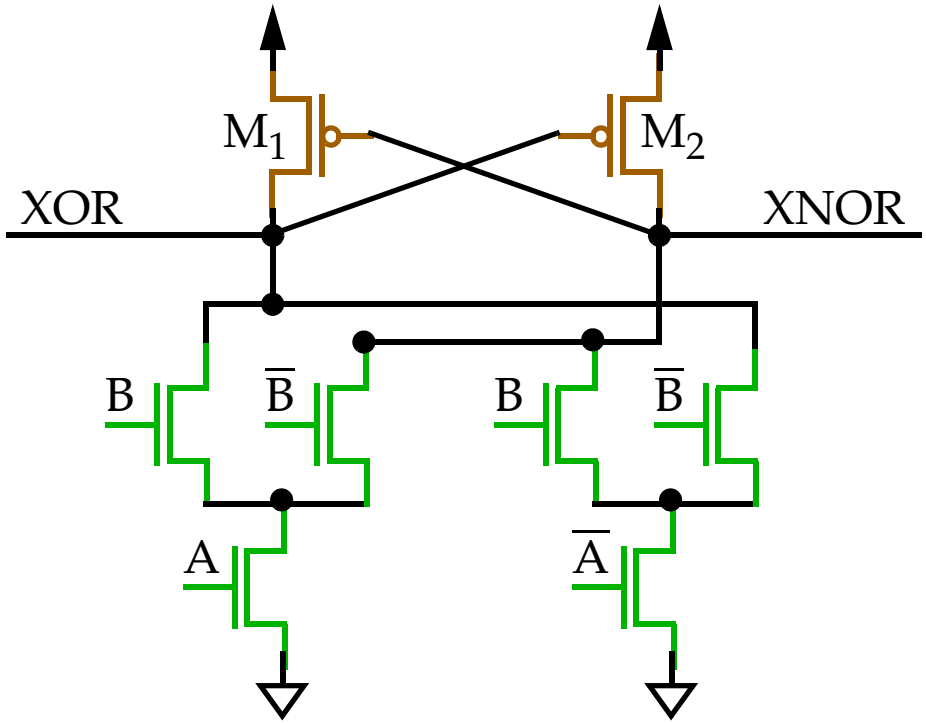
This in turn, shuts off M_1.

Speed advantage of pseudo-NMOS (reduced output parasitics) with *no static power consumption*, but occupies **extra area**.

Ratioed Logic

- Even better loads (cont)

  However, transistors can be shared between PDN_1 and PDN_2.



This gate has been used to implement fast error-correcting logic in memories.

Plus, the availability of complementary signals eliminate extra inverter stages.