Process Variations

The parameters of individual transistors vary from:

- **Lot to lot** (interprocess variation)
- **Wafer to wafer** (interprocess variation)
- **Die to die** (intraprocess variation)

The observed random distribution of *identically drawn* devices is caused by:

- Variations in process parameters, e.g.,
  - Impurity concentration densities
  - Oxide thicknesses
  - Diffusion Depths

These result from non-uniform conditions during the deposition and/or the diffusion of the impurities (dopants).

Changes in these parameters cause electrical parameters to vary, such as sheet resistance and threshold voltage.

Process Variations

Causes for observed random distribution (cont):

- Variations in the dimensions of the devices:

  Limited resolution of the photolithographic process which causes W/L variations in MOS transistors.

Many design parameters are totally uncorrelated.

Variations in MOS transistor length are unrelated to variations in V_T.

Observations:

- Process variations impact the parameters that determine circuit performance, e.g., transistor current.

- V_T can vary due to (1) changes in oxide thickness, (2) substract, polysilicon and implant impurity levels and (3) surface charge.

  Accurate control of V_T is very important.

  In the past, it varied up to 50% while today is is controlled within 25-50 mV.

Process Variations

- The main cause of variations in process transconductance, k'_n is changes in oxide thickness.

- Variations in W and L are caused by the lithographic process.
  These variations are not correlated because W is determined in the field oxide step while L is defined in the poly and src/drain diffusion steps.

These variations results in dramatic changes in device performance characteristics, in positive and negative directions.

This effects the design process, since your design is constrained by a specification, e.g., has to run at 3 GHz.

In order to account for these variations, you may design your circuit using **worst case** values for all device parameters.

Process Variations

While safe, this approach is prohibitively conservative and results in severely **over**designed and hence uneconomical circuits.

Manufacturer usually helps by providing *fast* and *slow* as well as *nominal* device models.

An Example: Consider the performance impact of variations on an NMOS transistor in a 0.25 μm CMOS process.

Assume that the device is in saturation with $V_{GS} = V_{DS} = 2.5$ V.

This produces a drain current of 220 mA.

The fast and slow models produce the following values:

fast: I_D = 265 mA (+20%)

slow: I_D = 182 mA (-17%)

Here, W and L are modified by +/- 10%, V_T by +/- 60mV and oxide thickness by (+/- 5%).

Process Variations

Process variations are not the only source of variation that impacts performance.

Variations in the power supply voltage can occur as well. A 10% variations can be expected.

fast: V_{DD} = 2.75 V: I_D = 302 mA (+37%)

slow: V_{DD} = 2.2.5 V: I_D = 155 mA (-30%)

This illustrates that the current levels, and therefore the performance, can vary by as much as 100% over the extremes.

In order to guarantee that the fabricated circuits meet performance requirements, under all circumstances, we need to make the transistor 42% (220 mA/155 mA) wider.

This results in a severe area penalty.

Process Variations

Fortunately, it is rare for all parameters to assume their worst (or best-case) values.

Most designs will display a performance centered around the nominal design.

Design for Manufacturability

Objective is to *center the design* so that the majority of the fabricated circuit (99%) fall within the performance specifications, while keeping the area overhead minimal.

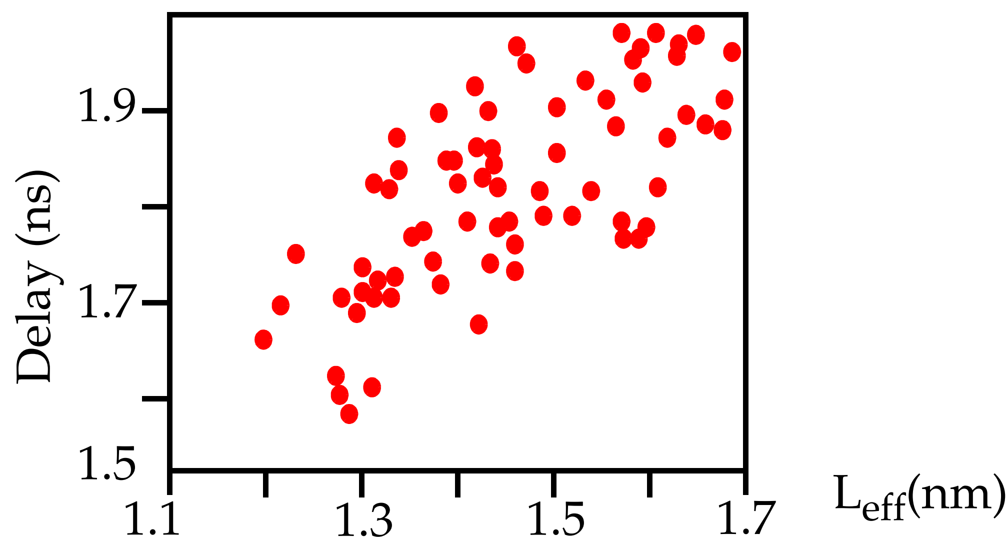
Tools are available to help with this.

Monte Carlo analysis involves simulating a circuit over a wide range of randomly chosen device parameters.

The result is a distribution plot of design constraints (delay or noise sensitivity) that help determine if the nominal design is economically viable.

Process Variations

For example, the impact of effective transistor channel length on the speed of an adder cell.



Therefore SPICE simulations should be taken with a grain of salt.

The device parameters used in the model are often *lot-averaged* results.

In other words, these parameters are **mean** values and individual device parameters will vary statistically around these values.

Process Variations

Modeling inaccuracies and power supply variations are two sources of variation between actual and simulated device performances.

Yet a third source of performance variation is **temperature**.

Don't waste your time tweaking picoseconds out of your design using SPICE.