Two cycles of Reset = 1, followed by a read request at address 00000000, that causes a read miss.

19 clock cycles needed for read miss.

Reset
Read at address 0x00
Data read from 0x00
Busy goes low

Busy goes high
Miss, send memory address and memory enable
1st data byte after 8 cycles
2nd data byte after 2 cycles

All bytes written
Write to 0x03, block already in cache due to the read miss, write data 0xFF
Read from 0x03, data written above
Write to 0xFF, block not in cache, causes a miss, write data 0xAA, no change in cache data, no need to access memory

**Project Waveforms: WRITE HIT/ READ HIT/ WRITE MISS**

- Write at address 0x03, data 0xFF
  - Busy goes high
  - Busy low after 2 clocks
  - 3 clock cycles needed for write hit
- Read from 0x03
  - Busy goes high
  - Busy low after 1 clock
  - Data available
- Write at address 0xFF, data 0xAA
  - Busy goes high
  - Busy low after 2 clocks
  - 3 clock cycles needed for write miss