Memory Types

Two basic types:
- **ROM**: Read-only memory
- **RAM**: Read-Write memory

Four commonly used memories:
- ROM
- Flash, EEPROM
- Static RAM (SRAM)
- Dynamic RAM (DRAM), SDRAM, RAMBUS, DDR RAM

Generic pin configuration:
Memory Chips

The number of address pins is related to the number of memory locations. Common sizes today are 1K to 256M locations. Therefore, between 10 and 28 address pins are present.

The data pins are typically bi-directional in read-write memories. The number of data pins is related to the size of the memory location. For example, an 8-bit wide (byte-wide) memory device has 8 data pins. Catalog listing of 1K X 8 indicate a byte addressable 8K bit memory with 10 address pins.

Each memory device has at least one chip select (CS) or chip enable (CE) or select (S) pin that enables the memory device. This enables read and/or write operations. If more than one are present, then all must be 0 in order to perform a read or write.
Memory Chips

Each memory device has at least one control pin.
For ROMs, an output enable (OE) or gate (G) is present.
The OE pin enables and disables a set of tristate buffers.
For RAMs, a read-write (R/W) or write enable (WE) and read enable (OE) are present.
For dual control pin devices, it must be hold true that both are not 0 at the same time.

ROM:
Non-volatile memory: Maintains its state when powered down.
There are several forms:
- **ROM**: Factory programmed, cannot be changed. Older style.
- **PROM**: Programmable Read-Only Memory.
  Field programmable but only once. Older style.
- **EPROM**: Erasable Programmable Read-Only Memory.
  Reprogramming requires up to 20 minutes of high-intensity UV light exposure.
Memory Chips

ROMs (cont):

- **Flash, EEPROM**: Electrically Erasable Programmable ROM. Also called **EAROM** (Electrically Alterable ROM) and **NOVRAM** (NOn-Volatile RAM).
  Writing is much slower than a normal RAM.

Used to store setup information, e.g. video card, on computer systems. Can be used to replace EPROM for BIOS memory.
EPROMs

Intel 2716 EPROM (2K X 8):

V_{PP} is used to program the device by applying 25V and pulsing PGM while holding \overline{CS} high.

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<table>
<thead>
<tr>
<th>Pin(s)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_0-A_10</td>
<td>Address</td>
</tr>
<tr>
<td>PD/PGM</td>
<td>Power down/Program</td>
</tr>
<tr>
<td>CS</td>
<td>Chip Select</td>
</tr>
<tr>
<td>O_0-O_7</td>
<td>Outputs</td>
</tr>
</tbody>
</table>

2K x 8 EPROM
**EPROMs**

2716 Timing diagram:

Sample of the data sheet for the 2716 A.C. Characteristics.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ.</td>
</tr>
<tr>
<td>t_{ACC1}</td>
<td>Addr. to Output Delay</td>
<td>250</td>
<td>450</td>
</tr>
<tr>
<td>t_{OH}</td>
<td>Addr. to Output Hold</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>t_{DF}</td>
<td>Chip Deselect to Output Float</td>
<td>0</td>
<td>100</td>
</tr>
</tbody>
</table>

This EPROM requires a wait state for use with the 8086 (460ns constraint).
**SRAMs**

**TI TMS 4016 SRAM (2K X 8):**

![Diagram of TMS4016 SRAM](image)

- **Pin(s)** | **Function**
  - A0-A10 | Address
  - DQ0-DQ7 | Data In/Data Out
  - S (CS) | Chip Select
  - G (OE) | Read Enable
  - W (WE) | Write Enable

Virtually identical to the EPROM with respect to the pinout.

However, access time is faster (250ns).

See the timing diagrams and data sheets in text.

SRAMs used for caches have access times as low as 10ns.
**DRAMs**

**DRAM:**

SRAMs are limited in size (up to about 128K X 8).

DRAMs are available in much larger sizes, e.g., 64M X 1.

DRAMs MUST be refreshed (rewritten) every 2 to 4 ms

Since they store their value on an integrated capacitor that loses charge over time.

This refresh is performed by a special circuit in the DRAM which refreshes the entire memory.

Refresh also occurs on a normal read or write.

More on this later.

The large storage capacity of DRAMs make it impractical to add the required number of address pins.

Instead, the address pins are *multiplexed.*
**DRAMs**

**TI TMS4464 DRAM (64K X 4):**

<table>
<thead>
<tr>
<th>Pin(s)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A₀-A₇</td>
<td>Address</td>
</tr>
<tr>
<td>DQ₀-DQ₃</td>
<td>Data In/Data Out</td>
</tr>
<tr>
<td>RAS</td>
<td>Row Address Strobe</td>
</tr>
<tr>
<td>CAS</td>
<td>Column Address Strobe</td>
</tr>
<tr>
<td>G</td>
<td>Output Enable</td>
</tr>
<tr>
<td>W</td>
<td>Write Enable</td>
</tr>
</tbody>
</table>

The TMS4464 can store a total of 256K bits of data.

It has **64K** addressable locations which means it needs **16** address inputs, but it has only **8**.

The row address (A₀ through A₇) are placed on the address pins and strobed into a set of internal latches.

The column address (A₈ through A₁₅) is then strobed in using CAS.
TI TMS4464 DRAM (64K X 4) Timing Diagram:

CAS also performs the function of the chip select input.

Address BUS

74157 (2-to-1MUX)  S

0: latch A to Y
1: latch B to Y

Inputs to DRAM

RAS

74157 (2-to-1MUX)  S
**DRAMs**

Larger DRAMs are available which are organized as $1M \times 1$, $4M \times 1$, $16M \times 1$, $64M \times 1$, $256M \times 1$.

DRAMs are typically placed on SIMM (Single In-line Memory Modules) boards. **30-pin** SIMMs come in $1M \times 8$, $1M \times 9$ (parity), $4M \times 8$, $4M \times 9$.

**72-pin** SIMMs come in $1/2/3/8/16M \times 32$ or $1M \times 36$ (parity).
**Memory**

Pentiums have a 64-bit wide data bus.

The **30-pin** and **72-pin** SIMMs are not used on these systems.

Rather, **64-bit DIMMs (Dual In-line Memory Modules)** are the standard.

These organize the memory 64-bits wide.

The board has DRAMs mounted on both sides and is **168** pins.

Sizes include **2M X 64** (**16M**), **4M X 64** (**32M**), **8M X 64** (**64M**) and **16M X 64** (**128M**).

The DIMM module is available in **DRAM**, **EDO** and **SDRAM** (and **NVRAM**) with and without an EPROM.

The EPROM provides information about the size and speed of the memory device for PNP applications.