CMSC 313 Lecture 25

- Registers
- Memory Organization
- DRAM
Four-Bit Register

- Makes use of tri-state buffers so that multiple registers can gang their outputs to common output lines.
Left-Right Shift Register with Parallel Read and Write

<table>
<thead>
<tr>
<th>Control</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>$c_1$</td>
<td>$c_0$</td>
</tr>
<tr>
<td>0  0</td>
<td>No change</td>
</tr>
<tr>
<td>0  1</td>
<td>Shift left</td>
</tr>
<tr>
<td>1  0</td>
<td>Shift right</td>
</tr>
<tr>
<td>1  1</td>
<td>Parallel load</td>
</tr>
</tbody>
</table>

- $c_0$: Enable (EN)
- $c_1$: Control Function
- $D$: D Flip-Flop
- $Q$: Output
- $CLK$: Clock
- $D_3$, $D_2$, $D_1$, $D_0$: Data Inputs
- $Q_3$, $Q_2$, $Q_1$, $Q_0$: Shift Register Outputs
Example of Multiplication Using Serial Multiplier

Multiplicand (M):

C
0
Α
0 0 0 0 0
Q
1 0 1 1

0 1 1 0 1 1 0 1 1 Add M to A
0 0 1 1 0 1 1 0 1 Shift
1 0 0 1 1 1 1 0 1 Add M to A
0 1 0 0 1 1 1 0 0 Shift
0 0 1 0 0 1 1 1 1 Shift (no add)
1 0 0 0 1 1 1 1 1 Add M to A
0 1 0 0 0 1 1 1 1 Shift

Product
Functional Behavior of a RAM Cell

Diagram:
- **Read**
- **Select**
- **Data In/Out**
- **D**
- **Q**
- **CLK**

Diagram features logic gates and connections to represent the functional behavior of a RAM cell.
Simplified RAM Chip Pinout

A<sub>0</sub>-A<sub>m-1</sub>  \rightarrow  \text{Memory Chip}  \rightarrow  D<sub>0</sub>-D<sub>w-1</sub>

WR

CS
A Four-Word Memory with Four Bits per Word in a 2D Organization
A Simplified Representation of the Four-Word by Four-Bit RAM
2-1/2D Organization of a 64-Word by One-Bit RAM

Two bits wide: One bit for data and one bit for select.
Decoder

\[
D_0 = \overline{A} \overline{B} \quad D_1 = \overline{A} B \quad D_2 = A \overline{B} \quad D_3 = A B
\]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Enable = 1</th>
<th>D_0</th>
<th>D_1</th>
<th>D_2</th>
<th>D_3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0 0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0 1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1 0</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>1</td>
<td>1 1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Enable = 0</th>
<th>D_0</th>
<th>D_1</th>
<th>D_2</th>
<th>D_3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0 1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1 0</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1 1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Two Four-Word by Four-Bit RAMs are Used in Creating a Four-Word by Eight-Bit RAM

![Diagram of two four-word by four-bit RAMs connected to form a four-word by eight-bit RAM.]

- CS (Chip Select) inputs are connected to select the appropriate RAM.
- WR (Write) input controls the writing operation.
- A0 and A1 are the address inputs, determining the specific memory location.
- D7, D6, D5, D4 are the data inputs to the left 4x4 RAM.
- D3, D2, D1, D0 are the data inputs to the right 4x4 RAM.
- Q7, Q6, Q5, Q4 are the data outputs from the left 4x4 RAM.
- Q3, Q2, Q1, Q0 are the data outputs from the right 4x4 RAM.
Two Four-Word by Four-Bit RAMs Make up an Eight-Word by Four-Bit RAM
Single-In-Line Memory Module

- Adapted from (Texas Instruments, MOS Memory: Commercial and Military Specifications Data Book, Texas Instruments, Literature Response Center, P.O. Box 172228, Denver, Colorado, 1991.)

PIN NOMENCLATURE

<table>
<thead>
<tr>
<th>PIN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A9</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>CAS</td>
<td>Column-Address Strobe</td>
</tr>
<tr>
<td>DQ1-DQ8</td>
<td>Data In/Data Out</td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
</tr>
<tr>
<td>RAS</td>
<td>Row-Address Strobe</td>
</tr>
<tr>
<td>Vcc</td>
<td>5-V Supply</td>
</tr>
<tr>
<td>Vss</td>
<td>Ground</td>
</tr>
<tr>
<td>W</td>
<td>Write Enable</td>
</tr>
</tbody>
</table>
Types of Random Access Memory

• **Static RAM (SRAM)**
  - Each bit is stored in a type of flip-flop
  - Typically takes four or six transistors per bit
  - Faster, but takes up more space in a chip
  - Retains information as long as power is supplied
  - Not to be confused with flash memory in digital cameras (EEPROMs)

• **Dynamic RAM (DRAM)**
  - Each bit is stored in a capacitor
  - Uses one capacitor and one transistor per bit
  - Slower, but takes up less space in a chip
  - Must be refreshed periodically (milliseconds), since the capacitor leaks
• A DRAM memory cell

Word Line

Capacitor

GND

Bit Line

• Word line selects cell for reading or writing
• To write, the bit line is charged with logic 1 or 0
• To read, sensitive amplifier circuits detect small changes in bit line.
• Reading discharges the capacitor.
DRAM Read Cycle

1. Row address placed on the address bus.
2. Row Address Strobe (RAS) is asserted, allowing the row address to latch.
3. Row address decoder selects proper row.
4. Write Enable (WE) disabled.
5. Column address placed on the address bus.
6. Column Address Strobe (CAS) is activated, allowing the column address to latch.
7. Once the CAS signal has stabilized, sensing amplifiers places data from the selected row & column on data bus.
8. RAS and CAS deactivated. Cycle begins again.
DRAM

• DRAM is asynchronous, ignores system bus clock.
  ◦ tRAC = Row Access Time = delay from RAS assertion until data is ready
  ◦ tCAC = Column Access Time = delay from CAS assertion until data is ready

• DRAM access is slooooooow

• Each memory access must wait for time it takes to activate and deactivate RAS.

• Fast Page Mode (FPM) DRAM allows successive reads from the same row without deactivating RAS.

• Extended Data Out (EDO) DRAM overlaps CAS assertion and data reads.
Fast Page Mode Read

RAS: RAS Active

CAS: Precharge, CAS Active, Precharge, Precharge, Precharge

Address Bus: Row, Col. 1, Col. 2, Col. 3, Col. 4

WE: x

Data Bus: tRAC, Data 1, tCAC, D2, tCAC, D3, tCAC, D4
EDO Read

RAS: RAS Active

CAS: Precharge, CAS, Pre, Pre, Pre, Pre, Pre, Pre

Address Bus: Row, Col. 1, Col. 2, Col. 3, Col. 4, Col. 5, Col. 6

WE:

data Bus: tRAC, tCAC, Data 1, D2, D3, D4, D5, tCAC, tCAC, tCAC, tCAC, tCAC, tCAC, tCAC
Synchronous DRAM (SDRAM)

• Uses system bus clock.

• Current models run at 433MHz (still much slower than CPU).

• Burst mode allows fast successive reads from the same row. (Good way to read in a cache line!)

• Double Data Rate (DDR) SDRAM provides data on the positive and negative edges of the clock.
Next Time

- Cache Memory