CMSC 313 Preview Slides

These are draft slides.
The actual slides presented in lecture may be different due to last minute changes, schedule slippage, ...
CMSC 313 Lecture 26

• Registers
• Memory Organization
• DRAM
Four-Bit Register

- Makes use of tri-state buffers so that multiple registers can gang their outputs to common output lines.
Left-Right Shift Register with Parallel Read and Write

<table>
<thead>
<tr>
<th>Control</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>c_1 c_0</td>
<td></td>
</tr>
<tr>
<td>0 0</td>
<td>No change</td>
</tr>
<tr>
<td>0 1</td>
<td>Shift left</td>
</tr>
<tr>
<td>1 0</td>
<td>Shift right</td>
</tr>
<tr>
<td>1 1</td>
<td>Parallel load</td>
</tr>
</tbody>
</table>
A Serial Multiplier

Multiplicand (M)

\[
\begin{array}{c}
m_3 \ m_2 \ m_1 \ m_0
\end{array}
\]

4-Bit Adder

Add

Shift Right

Multiplier (Q)

\[
\begin{array}{c}
q_3 \ q_2 \ q_1 \ q_0
\end{array}
\]

Shift and Add Control Logic

A Register

\[
\begin{array}{c}
a_3 \ a_2 \ a_1 \ a_0
\end{array}
\]
Example of Multiplication Using Serial Multiplier

<table>
<thead>
<tr>
<th>C</th>
<th>A</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>1011</td>
</tr>
</tbody>
</table>

Initial values

<table>
<thead>
<tr>
<th>Multiplicand (M):</th>
<th>1101</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1101 1011</td>
<td></td>
</tr>
<tr>
<td>0 0110 1101</td>
<td></td>
</tr>
<tr>
<td>1 0011 1101</td>
<td></td>
</tr>
<tr>
<td>0 1001 1110</td>
<td></td>
</tr>
<tr>
<td>0 0100 1111</td>
<td></td>
</tr>
<tr>
<td>1 0011 1111</td>
<td></td>
</tr>
<tr>
<td>0 1000 1111</td>
<td></td>
</tr>
</tbody>
</table>

Product
Functional Behavior of a RAM Cell

Diagram:

- **Select**
  - Input to latch
- **Read**
  - Output from latch
  - Controls data flow
- **Data In/Out**
  - Input and output for data
- **D, Q, CLK**
  - Latch components

Diagram labels:

- **D**
- **Q**
- **CLK**
- **Read**
- **Select**
- **Data In/Out**
Simplified RAM Chip Pinout

Memory Chip

\[ A_0 - A_{m-1} \quad \rightarrow \quad WR \quad \rightarrow \quad CS \quad \leftarrow \quad D_{0-D_{w-1}} \]
A Four-Word Memory with Four Bits per Word in a 2D Organization
A Simplified Representation of the Four-Word by Four-Bit RAM
2-1/2D Organization of a 64-Word by One-Bit RAM

Two bits wide:
One bit for data and
one bit for select.
Decoder

\[
D_0 = \overline{A} \overline{B} \\
D_1 = \overline{A} B \\
D_2 = A \overline{B} \\
D_3 = A B
\]

<table>
<thead>
<tr>
<th>Enable = 1</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A B</td>
<td>D_0</td>
<td>D_1</td>
<td>D_2</td>
<td>D_3</td>
</tr>
<tr>
<td>0 0</td>
<td>1 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>0 1 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>0 0 1 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>0 0 0 1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Enable = 0</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A B</td>
<td>D_0</td>
<td>D_1</td>
<td>D_2</td>
<td>D_3</td>
</tr>
<tr>
<td>0 0</td>
<td>0 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>0 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>0 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1</td>
<td>0 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Two Four-Word by Four-Bit RAMs are Used in Creating a Four-Word by Eight-Bit RAM
Two Four-Word by Four-Bit RAMs Make up an Eight-Word by Four-Bit RAM
Single-In-Line Memory Module

- Adapted from Texas Instruments, *MOS Memory: Commercial and Military Specifications Data Book*, Texas Instruments, Literature Response Center, P.O. Box 172228, Denver, Colorado, 1991.

### PIN NOMENCLATURE

<table>
<thead>
<tr>
<th>PIN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A9</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>CAS</td>
<td>Column-Address Strobe</td>
</tr>
<tr>
<td>DQ1-DQ8</td>
<td>Data In/Data Out</td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
</tr>
<tr>
<td>RAS</td>
<td>Row-Address Strobe</td>
</tr>
<tr>
<td>Vcc</td>
<td>5-V Supply</td>
</tr>
<tr>
<td>Vss</td>
<td>Ground</td>
</tr>
<tr>
<td>W</td>
<td>Write Enable</td>
</tr>
</tbody>
</table>

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**Adapted from** *Texas Instruments, MOS Memory: Commercial and Military Specifications Data Book*, Texas Instruments, Literature Response Center, P.O. Box 172228, Denver, Colorado, 1991.
Types of Random Access Memory

**• Static RAM (SRAM)**
- Each bit is stored in a type of flip-flop
- Typically takes four or six transistors per bit
- Faster, but takes up more space in a chip
- Retains information as long as power is supplied
- Not to be confused with flash memory in digital cameras (EEPROMs)

**• Dynamic RAM (DRAM)**
- Each bit is stored in a capacitor
- Uses one capacitor and one transistor per bit
- Slower, but takes up less space in a chip
- Must be refreshed periodically (milliseconds), since the capacitor leaks
- A DRAM memory cell

Word Line  
Capacitor  
GND  
Bit Line

- Word line selects cell for reading or writing
- To write, the bit line is charged with logic 1 or 0
- To read, sensitive amplifier circuits detect small changes in bit line.
- Reading discharges the capacitor.
DRAM Read Cycle

1. Row address placed on the address bus.
2. Row Address Strobe (RAS) is asserted, allowing the row address to latch.
3. Row address decoder selects proper row.
4. Write Enable (WE) disabled.
5. Column address placed on the address bus.
6. Column Address Strobe (CAS) is activated, allowing the column address to latch.
7. Once the CAS signal has stabilized, sensing amplifiers places data from the selected row & column on data bus.
8. RAS and CAS deactivated. Cycle begins again.
DRAM Read

- **RAS**: Precharge - RAS Active - Precharge
- **CAS**: Precharge - CAS Active - Precharge
- **Address Bus**: Row - Column - Row - Column
- **WE**:
- **Data Bus**: tRAC - Data - tRAC - Data
DRAM

• DRAM is asynchronous, ignores system bus clock.
  ◦ tRAC = Row Access Time = delay from RAS assertion until data is ready
  ◦ tCAC = Column Access Time = delay from CAS assertion until data is ready

• DRAM access is sloooooooow

• Each memory access must wait for time it takes to activate and deactivate RAS.

• Fast Page Mode (FPM) DRAM allows successive reads from the same row without deactivating RAS.

• Extended Data Out (EDO) DRAM overlaps CAS assertion and data reads.
Fast Page Mode Read

RAS
- RAS Active

CAS
- Precharge
- CAS Active
- Precharge
- Precharge
- Precharge

Address Bus
- Row
- Col. 1
- Col. 2
- Col. 3
- Col. 4

WE

Data Bus
- tRAC
- Data 1
- tCAC
- D2
- tCAC
- D3
- tCAC
- D4
- tCAC
Synchronous DRAM (SDRAM)

• Uses system bus clock.

• Current models run at 433MHz (still much slower than CPU).

• Burst mode allows fast successive reads from the same row. (Good way to read in a cache line!)

• Double Data Rate (DDR) SDRAM provides data on the positive and negative edges of the clock.
SDRAM Read

Clock

RAS

CAS

Address Bus

Row

Col.

BA0

WE

Data Bus

Data

Data

Data

Data

Data

DQM