CMSC 313 Preview Slides

These are draft slides.
The actual slides presented in lecture may be different
due to last minute changes, schedule slippage, ...
CMSC 313 Lecture 21

• Introduction to Sequential Logic
• Flip-Flops
Sequential Logic

- The combinational logic circuits we have been studying so far have no memory. The outputs always follow the inputs.
- There is a need for circuits with memory, which behave differently depending upon their previous state.
- An example is a vending machine, which must remember how many and what kinds of coins have been inserted. The machine should behave according to not only the current coin inserted, but also upon how many and what kinds of coins have been inserted previously.
- These are referred to as finite state machines, because they can have at most a finite number of states.
Classical Model of a Finite State Machine

- An FSM is composed of a combinational logic unit and delay elements (called flip-flops) in a feedback path, which maintains state information.
S-R Flip-Flop

- The S-R flip-flop is an active high (positive logic) device.

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<th>$R_i$</th>
<th>$Q_{i+1}$</th>
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Timing Behavior
NAND Implementation of S-R Flip-Flop
SR Latch using NAND GATES

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A Hazard

- It is desirable to be able to “turn off” the flip-flop so it does not respond to such hazards.

Principles of Computer Architecture by M. Murdocca and V. Heuring © 1999 M. Murdocca and V. Heuring
A Clock Waveform: The Clock Paces the System

- In a positive logic system, the “action” happens when the clock is high, or positive. The low part of the clock cycle allows propagation between subcircuits, so their inputs settle at the correct value when the clock next goes high.
Clocked S-R Flip-Flop

- The clock signal, CLK, enables the S and R inputs to the flip-flop.
Clocked D Flip-Flop

- The clocked D flip-flop, sometimes called a *latch*, has a potential problem: If D changes while the clock is high, the output will also change. The *Master-Slave* flip-flop (next slide) addresses this problem.
Master-Slave Flip-Flop

- The rising edge of the clock loads new data into the master, while the slave continues to hold previous data. The falling edge of the clock loads the new master data into the slave.

![Master-Slave Flip-Flop Diagram]

Timing Behavior:
- The rising edge of the clock loads new data into the master, while the slave continues to hold previous data. The falling edge of the clock loads the new master data into the slave.
Next Time

• Edge-triggered Flip Flops
• Introduction to Finite State Machines