

Review and AVR Architecture

Microcontrollers and AVR Specific Information

{micro} Processor, Computer, Controller

- CPU
 - Unit that fetches and processes a set of general-purpose instructions
- Microprocessor
 - A CPU on a single chip. It may also have other units (e.g. caches, floating point processing)
- Microcomputer
 - A microprocessor + I/O + memory+ etc are put together to form a small computer for applications like data collection, or control application.
- Microcontroller
 - A microcomputer on a single chip. It brings together the microprocessor core and a rich collection of peripherals and I/O capability.

Microcontroller (MCU)

- Common peripherals include
 - Serial communication devices
 - Timers, counters, pulse width modulators
 - Analog-to-digital and digital-to-analog convertors
- Particularly suited for use in embedded systems
 - Real-time control applications
 - On-chip program memory and devices
- Enables single-chip system implementation
 - Smaller and lower-cost products
- Examples: Motorola 68HC11xx, HC12xx, HC16xx, Intel 8051, 80251, PIC 16F84, PIC18, ARM9, ARM7, **Atmel AVR, etc.**

Alternatives for MCU

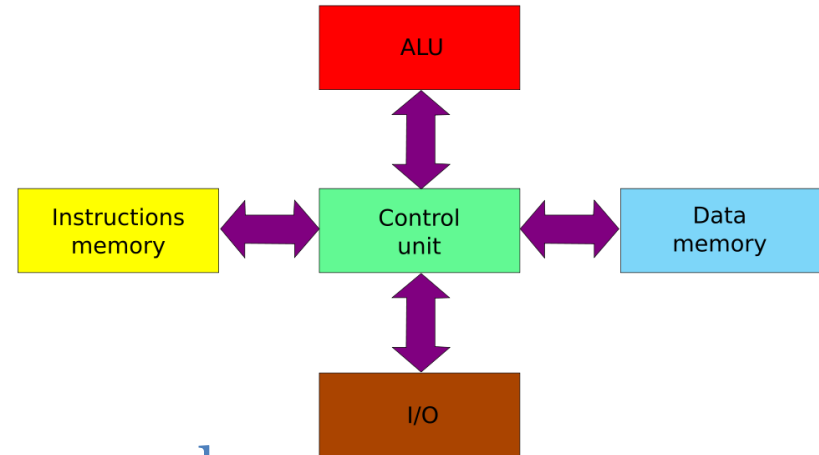
- Discrete ICs
 - Dedicated digital circuit
 - Can use various ICs for functions (AND, OR, etc..)
- PLD(Programmable Logic Device)
 - Contains various user selected logic functions
 - Results in more compact system compared to dedicated digital circuits
- ASIC(Application Specific Integrated Circuit)
 - Specific optimized implementation

Why use Microcontrollers?

- Peripheral loaded
 - ADC, DAC, GPIOs, Serial Interfaces
- Cheap
 - ~\$1 for 8-bit processor
- Low Power
 - ~300 μ A operation (1 AA battery for 275 days)
 - <1 μ A sleep (1 AA battery for 225 years)
- Programmable
 - Assembly or C

AVR Architecture

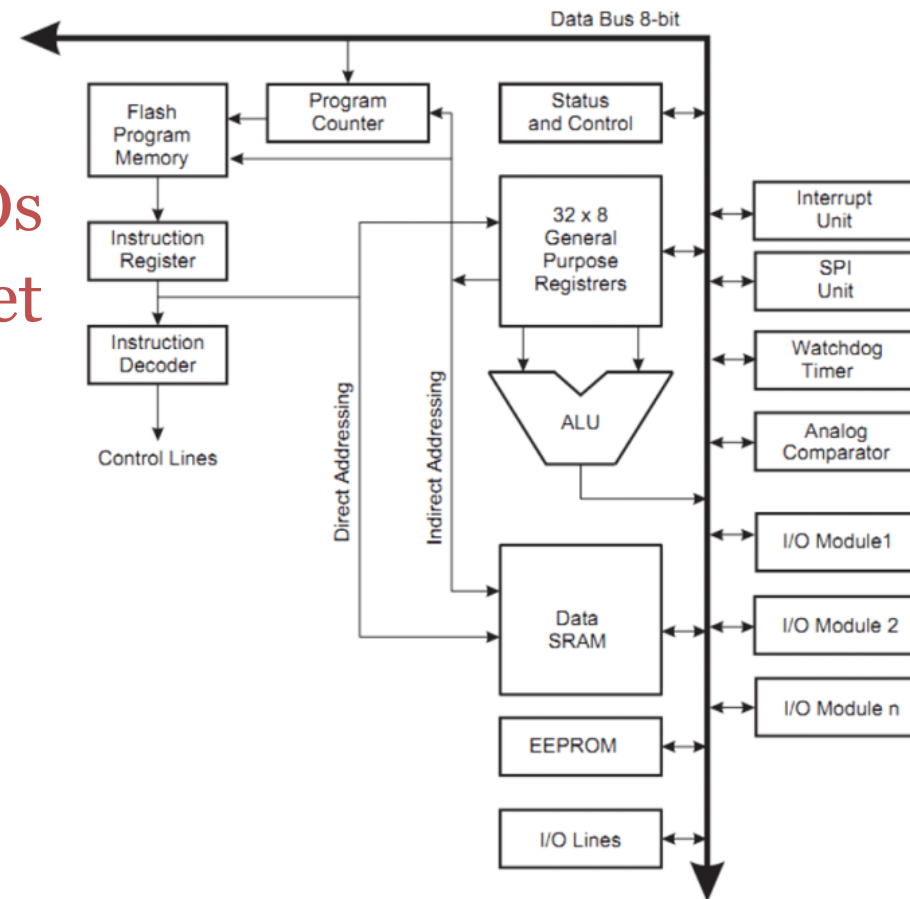
- RISC Harvard Architecture
 - RISC vs. CISC
 - Harvard vs. Von Neumann
 - Separate program and data memory bus
 - On-chip program memory → Flash memory
 - On-chip data memory → RAM and EEPROM
- 32 x 8 general purpose registers
- On-Chip programmable timers
- Internal and external interrupt sources
- Programmable watchdog timer
- On-chip RC clock oscillator
- Variety of I/O, Programmable I/O Lines



General 8-Bit AVR Architecture

- Models will differ in:
 - Memory size
 - Number and type of I/Os
 - Slightly in instruction set (hardware differences)
 - Power usage, voltage, clock

Figure 6-1. Block Diagram of the AVR Architecture

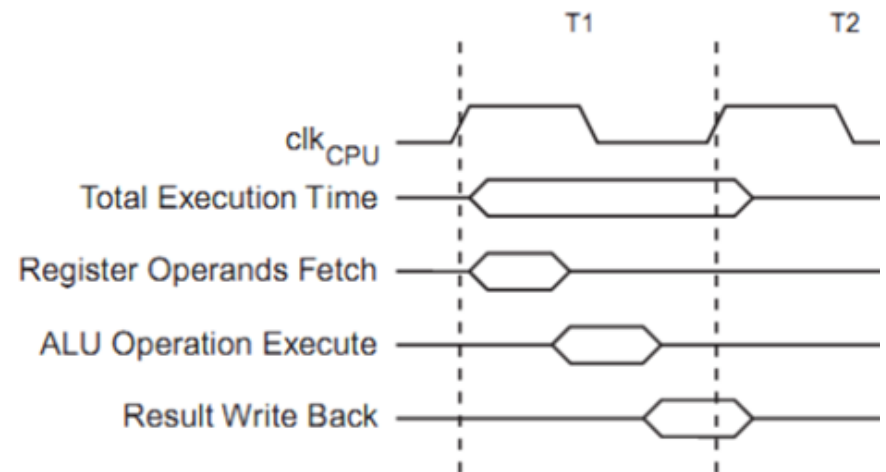


Pipeline

- AVR has 2-stage pipeline (Fetch, Execute)
 - Decode occurs in IF cycle
- Most instructions execute in a single clock cycle
 - Some take 2 or more cycles

		Clock Cycle					
Instruction		IF	EX				
			IF	EX			
				IF	EX		
					IF	EX	
						IF	EX
							IF

Figure 6-3. Single Cycle ALU Operation

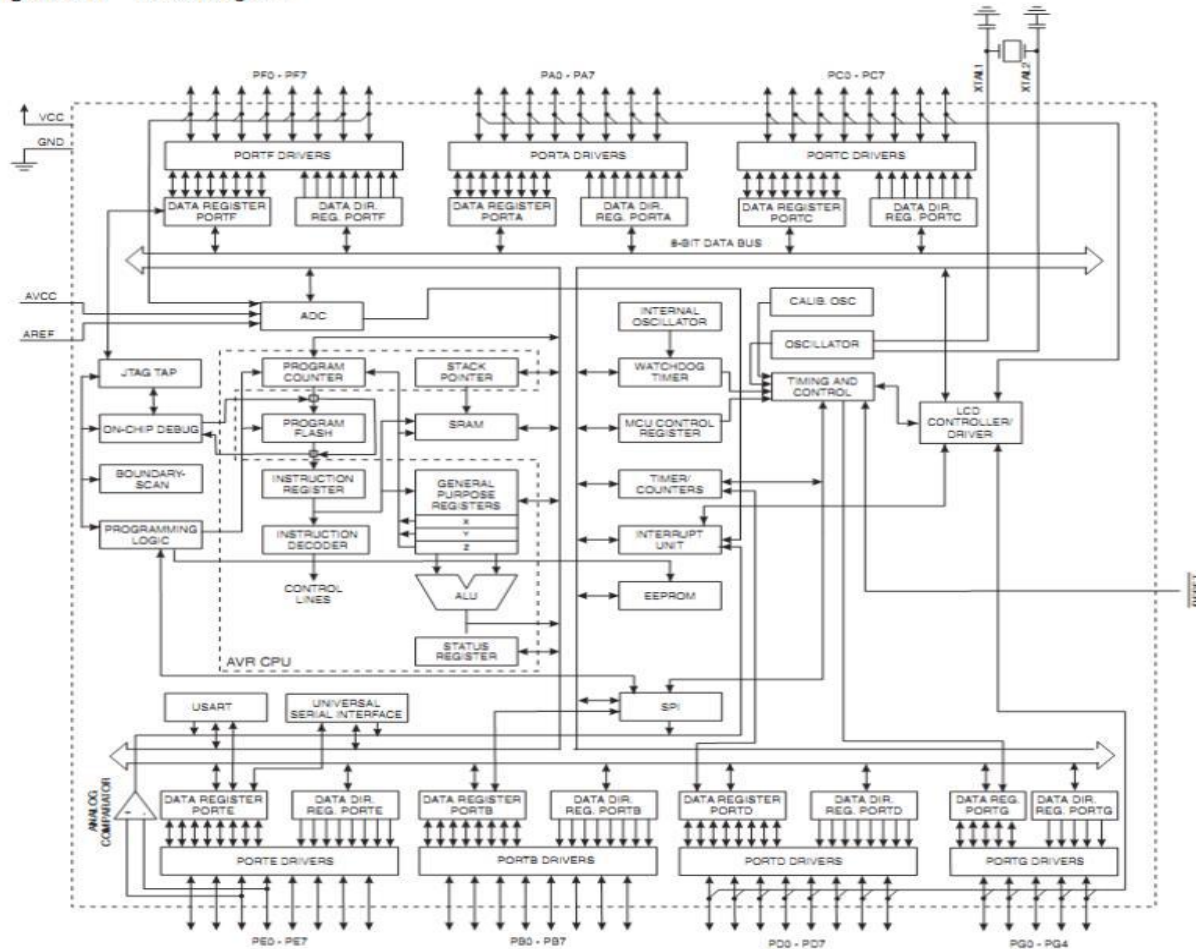


ATmega 169P

- Datasheet can be found at:
<http://www.atmel.com/Images/doc8018.pdf>
 - From megaAVR family
 - Families – Similar group of devices
 - “P” of 169P means “Low Power”
 - “16” in 169P means 16k program memory
 - “9” in 169P means 9th design revision

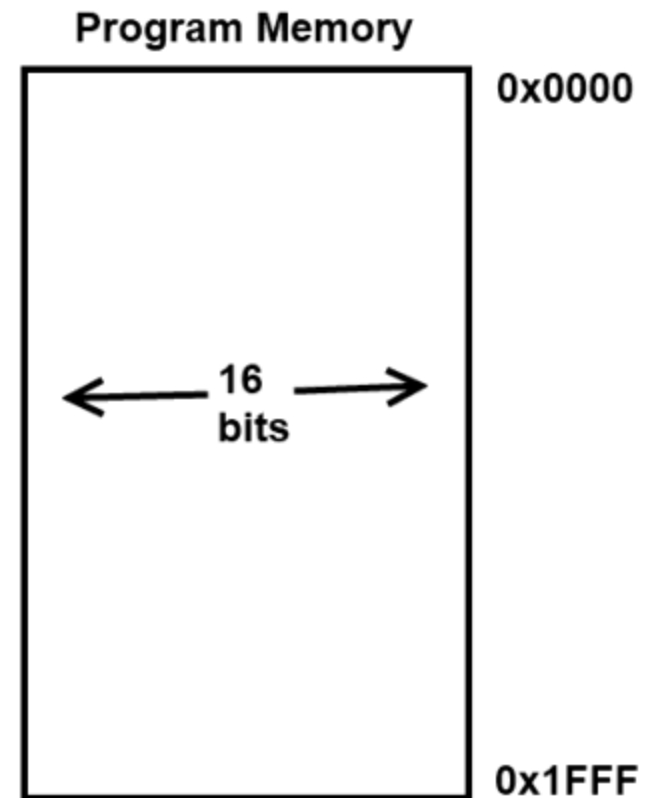
Atmega 169P

Figure 2-1. Block Diagram



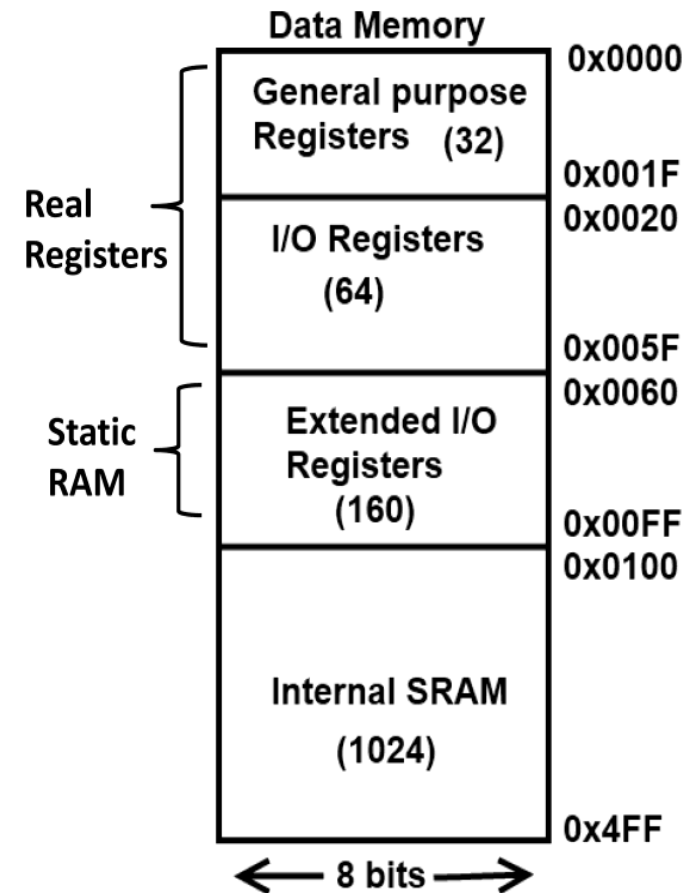
Program Memory

- Atmega 169P contains 16k bytes Flash memory
 - Program storage
- All AVR instructions are 16 or 32 bits wide
- Flash organized as 8k*16
- $8k = 2^{13} \rightarrow$ 13 bits needed to address program memory
 - Program Counter = 13 bits



Data Memory

- Entire data memory space can be accessed as memory
 - Register instructions faster on real registers
- General Purpose Registers
 - 32, labeled R0-R31
 - Called Register File
 - Can be used in instructions
 - i.e. ADD R2, R3

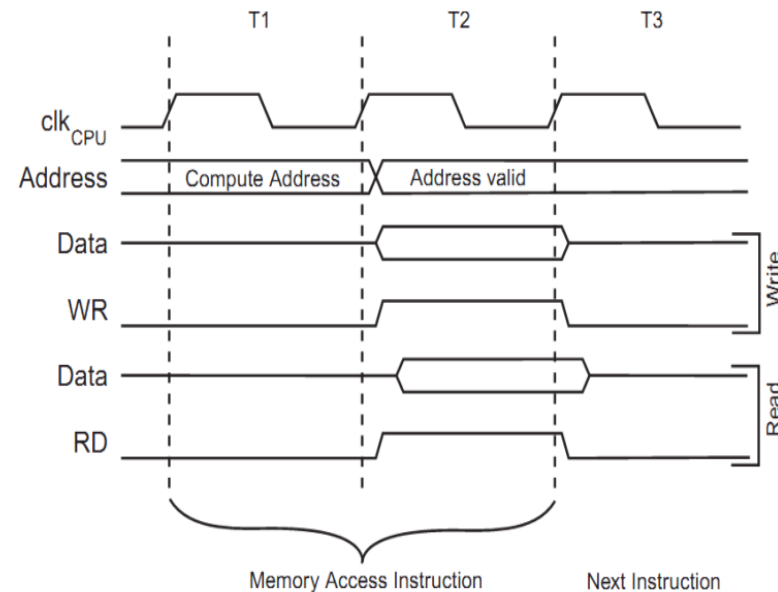


Special Function Registers (SFRs)

- SFRs include:
 - I/O Registers
 - Timers
 - Stack Pointers
 - Program Counter
- Some SFRs are not writeable by instructions
- I/O Registers
 - Can be accessed using LDs and STs
 - Some are bit accessible using SBI and CBI

SRAM Access Time

- 2 Cycles to access SRAM
- Address pointers (Registers X,Y,Z) used for addressing
- First Cycle
 - Register file accessed
 - ALU calculates address
- Second Cycle
 - Calculated address accesses SRAM location



EEPROM Space

- EEPROM
 - Electrically erasable programmable read-only memory
 - 100k write/erase cycles for a lifetime
 - 512 bytes
- Persists after power-down
- Reads and Writes will halt CPU