CSEE AI INITIATIVE

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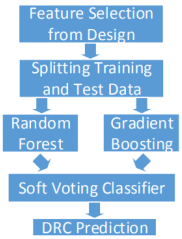
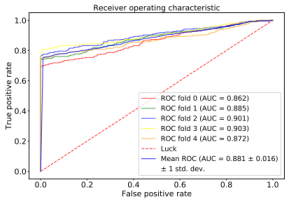
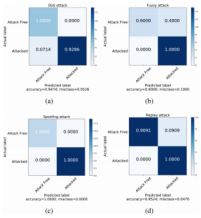
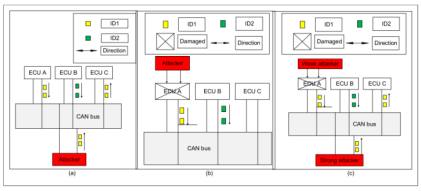
AI in IC Synthesis: At leading technology nodes, the industry faces a stiff challenge to make profitable ICs. The major issues are the design rule checking (DRC) violation, timing violations, area constraint, and frequency constraints. In this research, we cohort with the DARPA IDEA program that aims for "no-human-in-the-loop" and 24-hour turnaround time to implement an IC from design specifications. To reduce human effort, we introduce new machine learning algorithms to help inexperienced engineers. **Publications:** DAC 2019 and MWSCAS 2019.





AI in Network Security: The controller area network (CAN) is the most widely used intra-vehicular communication network in the automotive industry. Its simplicity in design lacks most of the requirements needed for a security-proven communication protocol. However, a safe and secure environment is imperative for autonomous as well as connected vehicles. Therefore CAN security is considered one of the essential topics in the automotive research community. In this research, we introduced novel graph-based machine learning algorithms to secure CAN bus. **Publications:** IEEE T-ITS 2020 and Springer JTS 2020.





AI-related Hardware: To enable real-time machine learning, we are working on an energy-efficient neuromorphic IC design.

~~IC design~~

Chen Chen Liu, Ph.D.

Abstract: Adapting to the new computing environment of artificial intelligence (AI) and Internet-of-Thing (IoT), our research efforts are devoting to high-performance intelligent computing in the domain of architecture and system, algorithm and applications via hardware and software cooperated solutions. The developments include brain-inspired computing approaches for ultra-high energy-efficient AI, novel deep learning algorithms, and algorithm-architecture co-designs for CPU/GPU systems acceleration and energy-efficiency optimization, federated learning and distributed systems, and their applications in autonomous driving, biomedical, *etc.*

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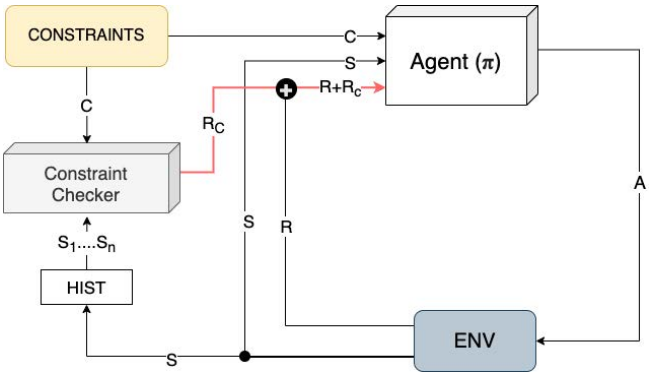
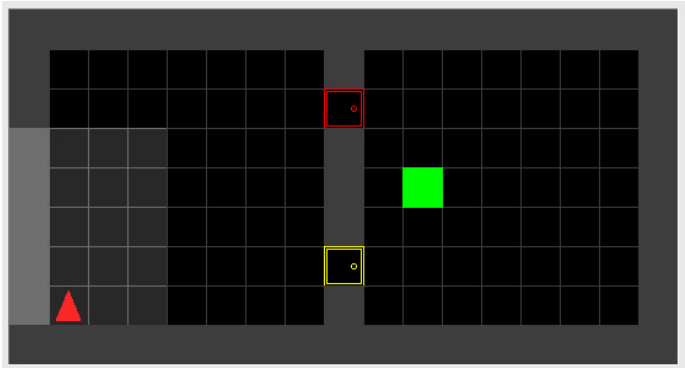
Guiding Safe Reinforcement Learning Policies Using Structured Language Constraints

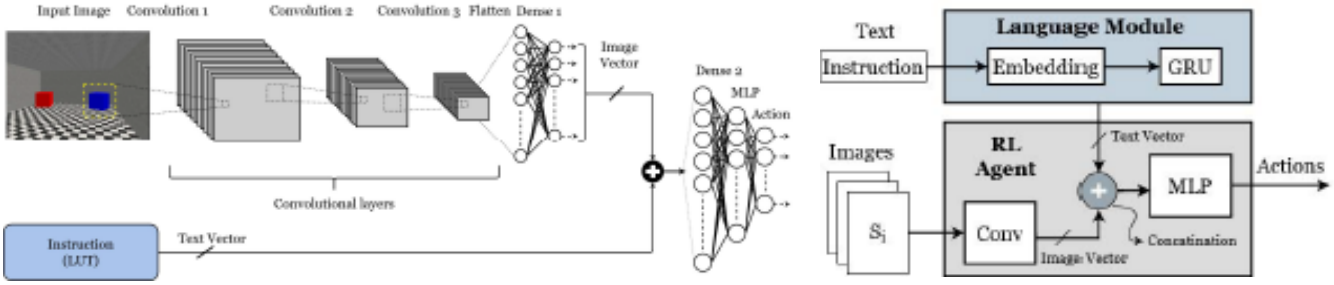
Reinforcement learning (RL) has shown success in solving complex sequential decision making tasks when a well defined reward function is available. For agents acting in the real world, these reward functions need to be designed very carefully to make sure the agents act in a safe manner. This is especially true when these agents need to interact with humans and perform tasks in such settings. However, hand-crafting such a reward function often requires specialized expertise and quickly becomes difficult to scale with task-complexity. This leads to the long-standing problem in reinforcement learning known as reward sparsity where sparse or poorly specified reward functions slow down the learning process and lead to sub-optimal policies and unsafe behaviors. To make matters worse, reward functions often need to be adjusted or re-specified for each task the RL agent must learn. On the other-hand, it's relatively easy for people to specify using language what you should or shouldn't do in order to do a task safely. Inspired by this, we propose a framework to train RL agents conditioned on constraints that are in the form of structured language, thus reducing effort to design and integrate specialized rewards into the environment. In our experiments, we show that this method can be used to ground the language to behaviors and enable the agent to solve tasks while following the constraints. We also show how the agent can transfer these skills to other tasks.





Energy-Efficient Hardware for Language Guided Reinforcement Learning

Reinforcement learning (RL) has shown great performance in solving sequential decision-making problems. While a lot of works have done on processing state information such as images, there has been some effort towards integrating natural language instructions into RL. In this research, we propose an energy-efficient architecture which is designed to receive both images and text inputs as a step towards designing RL agents that can understand human language and actin real-world environments. Different configurations are proposed to illustrate the trade-off between the number of parameters and the model accuracy, and a custom low power hardware is designed and implemented on FPGA based on the best configuration. The hardware designed to be configurable with different parameters such as the number of processing elements, so that it can easily balance power and performance. The high throughput configuration achieves 217 frames per second throughput with 1.2 mJ energy consumption per classification on Xilinx Artix-7 FPGA, while the low-power configuration consumes less than 139 mW for 30 frames per second classification. Compared to similar works using FPGA for hardware implementation, our design is more energy-efficient and needs less energy for generating each output.


Input Image
Convolution 1
Convolution 2
Convolution 3
Flatten
Dense 1
Image Vector
Convolutional layers
Instruction (LUT)
Text Vector
Dense 2
MLP
Action
Text
Instruction
Language Module
Embedding
GRU
Images
RL Agent
Text Vector
MLP
Actions
Conv
Image Vector
Concatination