

Alpha 21264

AlphaPowered

Alpha 21264 Microprocessor Product Brief

The Alpha 21264 microprocessor, with benchmarks over 30 SPECint95 and 50 SPECfp95, and with spectacular bandwidths over 3.2 GB/s for L2 cache and over 2.6 GB/s for memory, enables the system designer to produce the highest performance systems ranging from PC clients to enterprise servers. Systems implemented with Alpha microprocessors have been the industry's performance leaders since their introduction in 1992.

Applications

- Supports Windows NT—the world's fastest growing operating system.
 - The first Windows NT 64-bit platform.
 - Microsoft releases Windows NT applications concurrently for Alpha and Intel systems.
 - Runs non-native Windows NT applications using the DIGITAL FX!32 binary translator.
- Supports DIGITAL UNIX—the first 64-bit UNIX operating system.
- Supports OpenVMS Alpha — the powerful, scalable, and highly available operating system.
- Supports VxWorks and Linux/Alpha.
- Optimizes visual computing (video and 3D graphics) using its powerful floating-point unit and the new Alpha motion-video instructions (MVI). Supports real-time DVD authoring (MPEG2 and AC-3).
- Simplifies development of a single or dual Alpha 21264-based system using the 21272 core logic chipset.

Benefits

- System developers can deliver a 21264 solution that:
 - Exceeds end-user expectations in performance
 - Provides investment protection with a migration path to higher speed 21264s and future generations of Alpha microprocessors
 - Has multiple chip sources— Intel and Samsung
- The 21264 provides end users with a quantum leap in performance that:
 - Enables real-time visual computing
 - Performs instant data mining
 - Implements Internet commerce
 - Enhances medical imaging
 - Solves the most complex, large data-set problems quickly
 - Aids research centers in developing solutions to complex problems in disciplines such as medicine and polymers

Description

The 21264 is the third-generation 64-bit Alpha microprocessor. It includes the latest Alpha architecture extensions, such as motion-video instructions and byte/word operations.

The 21264 completely controls its L2 cache and provides flexible bus timing to support a range of L2 cache memory devices, such as:

- 200-MHz late-write SRAMs (3.2 GB/s)
- 166-MHz (333-MHz data rate) dual-data clock-forwarded SRAMs (5+ GB/s)

Pipeline Operation Sequence

The 21264 is a four-way out-of-order-issue microprocessor that performs dynamic scheduling, register renaming, and speculative execution. The 21264 pipeline contains four integer execution units. Two of the units can perform memory-address calculations for load and store operations. It also contains two floating-point execution units for add, divide, square root, and multiply functions.

The 21264 pipeline stages perform the following operations:

- Cycle 0—Instruction fetch using branch prediction.
- Cycle 1—Instruction data is transferred to the register rename map hardware.
- Cycle 2—Rename (map) instruction registers.
- Cycle 3—Issue instructions from the queues.
- Cycle 4—Read instruction registers.
- Cycle 5—Execute integer or floating-point instructions.
- Cycle 6—Write results to Dcache or register.

The bus interface unit, containing the memory and cache control units, maintains coherency between the Dcache and the L2 cache and main memory.

For More Information

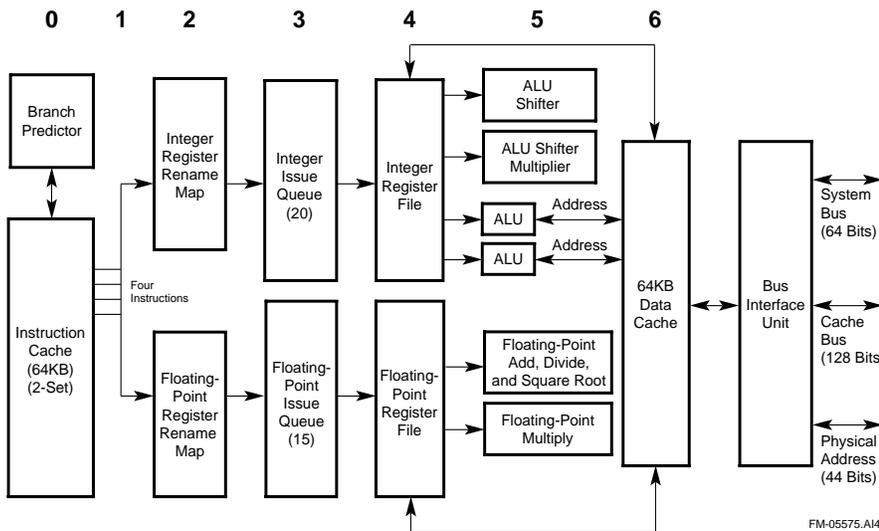
To learn more about the availability of the 21264, contact your local semiconductor distributor. To learn more about Digital Equipment Corporation's product portfolio, visit the Alpha OEM World Wide Web Internet site:

<http://www.digital.com/semiconductor/alpha/alpha.htm>

or, for general questions, you can contact the Alpha OEM Information Line at:

1-888-Alpha45 or
1-508-628-4865

Electronic mail address
alpha-oem@digital.com



Characteristics

Power supply	VSS = 0.0 V, VDD = 2.1 V min — 2.3 V max
Operating temperature	Tj = 100°C (212°F) maximum
Storage temperature range	-55°C to +125°C (-67°F to +257°F)
Package	588-pin pin grid array (PGA)
Transistor count	15.2 million
Process	0.35 micron CMOS six-layer metal
Die size	Approximately 3.1 cm ² (1.22 in ²)
Availability	Q4 1998

While DIGITAL believes the information in this publication is correct as of the date of publication, it is subject to change without notice.

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