Abstract

This technical report presents simulation results of experiments conducted on the ISCAS85 c432 benchmark circuit. The objective of these experiments is to determine the feasibility of a new device testing method called Transient Signal Analysis (TSA). TSA is based on an analysis of \( I_{DD} \) switching transients on the supply rails and voltage transients at selected test points. We present simulation experiments which show distinguishable characteristics between the transient waveforms of defective and non-defective devices. These variations are shown to exist for CMOS parametric, bridging and open defects, located both on and off of a sensitized path.

1.0 Introduction

Device testing is used to detect and/or diagnose defects introduced by the fabrication processes. Device logic testing analyzes the logical integrity of the device by using input test vectors which are a subset of all possible stimuli. However, these subsets are generated by techniques which are based on fault models that have been shown to be inadequate to detect all forms of CMOS defects [HSRF94][SH89][SMAM91]. Alternatively, parametric testing methods [Levi81][FTL90][DJRX90] are based on the analysis of a circuit’s parametric properties, for example, propagation delay, magnitude of supply current or transient response. While the algorithms for generating logic tests have been improved over time to handle more types of fault behaviors, parametric testing strategies offer intrinsically better solutions since they have been developed from the structural and electrical properties of CMOS circuits.

We propose a parametric testing method that uses the voltage transient behavior as well as the current transient behavior as a defect detection mechanism [PCL95]. While other parametric testing methods such as \( I_{DDQ} \) and \( I_{DD} \) testing methods take advantage of the global interconnection of devices to the power and ground supply rails, TSA additionally uses the transient voltage behavior of all primary outputs. Therefore, TSA implicitly captures delay fault information providing improvements on the resolution of current based approaches. Also, by using the transient signals from multiple test points simultaneously, TSA is able to use the cross correlation between these signals to distinguish between devices with parametric defects and those with catastrophic defects. This feature additionally provides TSA with a specifiable degree of process insensitivity reducing the occurrence of false positives in the defect detection process.

The remainder of this paper is organized as follows. In Section 2 we discuss CMOS defects and related research on device testing. Section 3 discusses the synthesis of the experimental circuit, c432. Section 4 presents the results of simulation experiments conducted on the c432. Section 5 gives a summary and conclusions.

2.0 Background and Motivation

Hawkins, et. al. [HNFG89] define a defect as a physical disorder at the device or interconnect level that may cause a logic gate to fail. Defects can cause catastrophic failures that appear under any operating condition or, as is common in CMOS ICs, failures may occur that are functions of clock rate, supply voltage (\( V_{DD} \)) and temperature [SH89]. The defects whose detections are dependent on the operating conditions of the IC are termed degradation or parametric faults. These parametric defects types can cause timing errors, noise margin reduction and excessive power consumption.

Both catastrophic and parametric defects and their corresponding faults need to be modeled in order to provide an accurate measure of defect coverage. CMOS defects that are difficult to detect using logical testing strategies are leakages, gate-oxide shorts, high-resistance bridges, source-drain shorts, floating gates and some types of open source or drain terminals [NM90]. Parametric testing methods are more effective in diagnosing these types of defects.

2.1 Shorting Defects

Many types of shorting defects are possible in
CMOS ICs and the location and surrounding topology determine the detectability of the short. Shorts can occur between metal lines and $V_{DD}$ or $V_{SS}(GND)$, between subnets as bridging defects and as gate oxide short circuits to the source, drain or channel region of the transistor. Midkiff and Bollinger have proposed a classification scheme for all the possibilities [MB91].

The only type of short guaranteed to be detected by a Single Stuck Fault (SSF) test set with 100% fault coverage is a low resistive short to $V_{DD}$ or $V_{SS}$. Shorts whose resistance can be ignored will be referred to a hard shorts. Resistive shorts will be used when the fault behavior depends on the resistance of the short and the way the fault is provoked [HM91].

A dominate source of failure in CMOS ICs is the gate oxide short (GOS) [HS85]. GOS defects can be caused by imperfections in a uniform growth pattern of the Thin Oxide layer or result from particulate contamination in the Thin Oxide mask [SH89]. A gate oxide short can also be created in post fabrication procedures by electrical overstress or electrostatic discharge or may develop later due to an effect called time dependent dielectric breakdown [RMSCR91].

An example of a gate oxide short is shown in Figure 1. The n-channel transistor of the middle inverter is shown with a GOS defect. Hawkins and Soden [HS85] performed a set of experiments on hardware versions of this circuit. Their results show that for the case studies where $V_{in}$ was driven high by the first inverter, the potentials at $V_{in}$ ranged from 6.8 Volts to the ideal 10 Volts. The low voltage at $V_{out}$ ranged from the ideal of 0 Volts to 2.11 Volts. However, for the case studies where $V_{in}$ was driven low, no significant variance from the ideal voltage behavior was noticeable. Several different types of resistive behavior were noted in the study. In cases where the induced defect was ohmic, resistances between 800 and 4.7k ohms were observed. These cases included shorts between the n-doped gate and the n+ source and drain regions. In other cases, non-linear I-V characteristics were observed. These cases included shorts between the n-doped gate and the channel region of the p-substrate (reversed-biased pn-junction) like the one shown in Figure 1. The test circuits were found to exhibit correct logical behavior in either case. However, when $V_{in}$ was driven high, a conducting path was created (shown by the arrows in the figure) between the power and ground rails. Under these test conditions, they noted an increase in steady-state current as well as an average increase of 13.6 percent in the rise and fall times of $V_{out}$. They conclude that the fault behavior of GOS defects depends on the location of the short (gate-to-channel vs. gate-to-source/drain region), the type of the transistor (n or p), the resistance of the short, and the state of the driving transistors (test pattern dependent).

Hao and McCluskey [HM91] support the conclusion that the fault behavior of GOS defects can in fact be test pattern dependent. They define a pattern dependent fault in a logic gate G as a fault whose expression is dependent not only on the inputs of G but also on the inputs to other gates. Figure 2 shows the circuit they used to illustrate pattern dependent fault behavior. In their experiments, a short was placed between the gate and source of a NAND gate transistor as shown by the shaded line between nodes y and c in the figure. They noted that the contention created by the second test pattern of $IJ = (10,11)$ would slow the falling transition of node y since the lowering of the voltage on line A would tend to shut transistor N1 off. However, they also noted that the type of fault observed at node y could be pattern sensitive since the generation of the logic 1 at node A could occur for three combinations of $IJ = (01,10,00)$. Using SPICE simulations, they modeled the short at 900 ohms (a resistive short) and demonstrated that the logic behavior of node y was different depending on whether the test sequence was $IJ = (000,001)$ or $(010,011)$. Only the second sequence with $IJ = 01$ generated a SA1 fault at y. With $IJ = 00$, the current drive through line A was sufficient to overcome the current...
drain through the resistive short. This allowed line \( A \) to pull-up to a voltage above \( N1 \)'s threshold voltage. With transistor \( N1 \) in a conducting state, line \( y \) discharged to a voltage below the threshold logic 0 voltage required by subsequent gates driven by \( y \) (NAND gate driving line \( Z \) in Figure 2). These results illustrate that the resistance of a GO5 as well as the strength of pull-up and pull-down paths play a role in the resulting fault behavior of the defect.

Bridging defects have also been shown to be a major source of failure in VLSI [FS88][LB91]. Bridging defects are defined by Ferguson, et. al. [FTL90] as undesired electrical connections between two or more lines in an IC resulting from extra conducting material or missing insulating material. Bridging defects may also develop after fabrication due to mechanisms including oxide surface conduction/lateral charge spreading and electromigration [SH89].

The detection of a low resistance bridging defect (one that causes a logical error) between independent subnets in an IC requires the state of the circuit to be set so that the fault is expressed and propagated to a PO. In order to create the fault condition, the test vector must set the shorted nodes to opposite logic polarities. In order to detect the fault, the test vector must also propagate the weaker, incorrect logic value, to a PO [MB91][FTL90].

A realistic fault model should consider three distinct fault behaviors. If a low resistive path exists between the bridged nodes and one node is able to dominate the other, a logical fault will occur at the weaker of the two nodes. If a resistive path exists across the bridge allowing the nodes to assume different potentials, then the fault may manifest itself as a delay fault along a sensitized path. If the resistance of the bridge is small enough, an \( I_{DDQ} \) fault may be detectable.

For low resistive bridging defects, a wired-AND or wired-OR fault model used in TTL and ECL technologies is not always applicable for CMOS. Storey and Maly [SM91] demonstrated this by showing an example (Figure 3) where the fixed relationship of wired-AND or wired-OR fault behavior fails to capture the actual behavior of a bridging defect. They determined that transistor sizes, transconductances and other technology and process parameters must be included in the model in order to predict the actual fault behavior. Their analysis shows that when \( ABCD = (1101) \), the bridge behaved like a wired-AND because both of the n-channel transistors in the NOR gate were turned on while only one of the p-channel transistors of the NAND gate was turned on. However, when the input was \( ABCD = (1000) \), the fault behavior changed to that predicted by a wired-OR model because both p-channel devices of the NAND gate were turned on while only one n-channel device of the NOR gate was turned on. This type of behavior was also verified by Soden and Hawkins on real ICs [SH89]. Soden, et. al. conclude that a parametric testing method is required in order to guarantee detection of the bridging defect under these circumstances.

Even when a wired-AND fault behavior is assumed, a logical test is not always possible since a test may not exist that causes a bridge to produce a logic fault. Furguson, et. al. [FTL90] demonstrated this possibility with the circuit and bridge shown in Figure 4. As indicated in the truth table on the right in the figure, only two input combinations make nodes \( w \) and \( x \) acquire different values; \( ABC = (011) \) and \( (110) \). They showed that in either case, the 0 dominated the D value on the other node but the output states of \( y \) or \( z \) were not affected since the NANDs driving these lines had the other input line \( (u \) or \( v) \) set to the dominating 0 state. This condition masked the
logic error that appeared on the bridged input line. They also noted that in spite of this, the presence of the defect would cause a delay at node Z for the input sequence $ABC = (010,011)$ since line $x$ would have to ‘fight’ line $w$’s logic 1 value.

Nigh and Maly [NM90] further illustrate this situation by showing that the bridge in Figure 5 changes only the dynamic behavior of the circuit. They noted that no combination of the inputs could cause nodes $x$ and $y$ to assume opposite potentials. However, when considering the case where $B = 1$ and $A$ transitioned from 0 to 1, they observed that transistor $N1$ would be required to discharge the capacitances of both nodes $x$ and $y$. This caused the 0 transition of node $x$ to be delayed proportional to the amount of additional capacitance that node $y$ contributed.

Rajsuman [Raj91][RJM91] analyzed the more complex case where a bridge created a feedback path in the circuit. He developed sufficient conditions for oscillation for resistive bridges that occurred across an odd number of inversions and showed that the propagation delay through the gates in the loop as well as the rise and fall times of these gates played a key role in determining the fault behavior of the bridge.

Other shorting defects include punch-through, parasitic transistor leakage, defective pn junctions and incorrect threshold voltages. Punch-through weakens the logic 0 and/or logic 1 output states and thus reduces noise margins. Parasitic transistor leakages include undesired pn junctions, bipolar and MOS transistors. Incorrect threshold voltage is primarily a result of fabrication process parameter variations in doping and oxide growth but also occur in post fabrication ICs as a result of charge instabilities. All of these defects can cause parametric faults including elevated $I_{DDQ}$ and increased propagation delay [SH89].

2.2 Open Defects

Opens in CMOS circuits are probably the most difficult of all CMOS flaws to detect using any of the current device testing techniques. A wide range of fault behavior has been observed and contradictions often arise as to the significance of parasitic capacitive coupling and the effect it has on the observed fault behavior. Opens or breaks can be caused by missing conducting material or by extra insulating material so that a single electrical node is separated into multiple nodes [FTL90]. An open circuit can occur in any of the interconnect materials affecting either the gate, drain or source connections. The fault behavior caused by the presence of an open is dependent on its location, its resistance, its width and the values of parasitic coupling capacitances and leakage currents associated with the floating node as well as the operating environment conditions.

The Stuck-Open fault model assumes that the width of the open is large enough to prevent AC parasitic capacitive coupling interactions between neighboring nodes. The effects of leakage currents is also ignored by the Stuck-Open fault model. Wadsack acknowledged the existence of leakage currents and the effect that they may have on making Stuck-Open faults timing sensitive [Wad78]. The application rate of the test vectors becomes another constraint when logic testing CMOS. Slow application rates may allow Stuck-Open faults to go undetected since leakage currents may have enough time to supply the output node with sufficient charge to make them appear correct when the sample is made.

Even when leakage currents are ignored and the width of the break is large, CMOS technology characteristic that make opens difficult to logic test reliably. Abraham, et. al. [AS85] discuss two such characteristics. Charge sharing refers to the redistribution of charge stored at an isolated node. This occurs when transistors adjacent to the isolated node are turned on allowing other isolated nodes charged to the opposite polarity to share the charge of the original node. Using the circuit shown in Figure 6 and the Stuck-Open test sequence $ABCD = (0111,1101)$ for the open shown between the n-channel transistors $N2$ and $N3$, they demonstrated that the effect of charge redistribu-
tion could affect the fault behavior at the output node. In their experiments, the initial test pattern set Out to 1 since transistor P1 was on and N1 was off. In addition, this vector set the grayed areas shown in Figure 6 to 0 Volts. The second vector tested the path between Out and GND through the n-channel transistors N1, N2 and N3. The open between N2 and N3 should have prevented Out from discharging to 0 Volts resulting in a Stuck-Open fault. However, the charge stored at Out was distributed among the circled areas when the second test pattern was applied. The final value as predicted by their model was 2.6 Volts. They contend that this value may not be interpreted by the gate driven by Out as a logic 1. Consequently, the defect would not be detected as a Stuck-Open fault. Also, since the resulting output voltage was near the switching point of an ideal CMOS inverter, the logical behavior of this fault may be operating environment sensitive.

They also show using the CMOS XOR gate shown in Figure 7 that path redundancy can be problematic for logic testing. In their experiment, they applied the test sequence AB = (00,01) to test the open defect shown in the figure. The first vector set node XNOR to a logic 1 through transistor P1. In this case, the transmission gate (N2/P2) was turned off preventing the transmission of A's logic 0 state to the node labeled XNOR. The second vector was supposed to turn on both gates of the pass transistor allowing A to drive the XNOR node to 0, primarily through transistor N2 since it alone could transmit a non-degraded 0. However, due to the open, the n-channel transistor was not activated. Therefore, p-channel transistors P1 and P2 were responsible for discharging the XNOR node. As a result, the XOR gate operated functionally correct due to the redundancy but was slower. Their simulations showed that the rise time of the output node, Out, increased from 2.2 nanoseconds to 8.5 nanoseconds. They concluded that a delay test is the only test strategy that will detect this type of fault behavior.

Other types of open defects cause only dynamic fault behavior. These types of defects are characterized by narrow opens (< 0.1um) or by the effects of parasitic capacitances and leakage currents on the open gate, source or drain of a transistor. For example, experimental evidence suggests that most open defects can not be treated as Stuck-Open faults [MNN88]. In particular, open gates to individual transistors can be influenced by the transistor’s internal capacitances. This interaction can effect the mode of operation of the defective device allowing it to operate correctly but suffer additional propagation delays. In addition, source opens of a transistor may also violate the assumptions of the Stuck-Open fault model. Leakages through the source and drain junctions can allow an output node to change state given enough time. The presence of visible light can influence the magnitude of the leakage currents dramatically.

A simulation study conducted by Rodriguez-Montanes et. al. [RMSCR91] using SPICE shows that capacitive coupling from adjacent metal lines to a floating gate can allow a transistor to conduct under the appropriate conditions. The experiment was conducted on the circuit shown in Figure 8. They show that a change in the voltage at node $V_{Metal}$ could invalidate a Stuck-Open test for inverter $INV_2$ due to the coupling capacitor $C_{mp}$. Since the node, $V_{Metal}$ is not considered explicitly in the generation of a Stuck-Open test for $INV_2$, they contend that the initialization vector may set $V_{Metal}$ to 0 in the process of initializing $V_{IN}$ to 1. They also contend that the second vector of the Stuck-Open test could set $V_{Metal}$ to 1 in the process.
of setting $V_{IN}$ to 0. Using these conditions, they have shown that the coupling interaction of capacitor $C_{mp}$ allowed the voltage applied to $V_{Metal}$ to charge the floating gate of transistor $N1$ above its threshold voltage. This allowed transistor $N1$ to conduct and mask the fault.

The experiments conducted by Henderson et al. [HSH91] contradict these results, however. The study examined the effects of electron tunneling across narrow openings ($< 0.1\mu m$) in CMOS inverter test chips. Open defects were introduced by controlled electromigration at gates connecting complementary transistor pairs. Gate capacitances significantly larger than the internal parasitic capacitances of the transistors allowed the inverters to experience long DC stability. For smaller gate capacitances, the floating gate acquired a DC voltage between $V_{DD}$ and $V_{SS}$ dependent on the parasitic capacitances and the leakage currents. More importantly, however, electron tunneling permitted DC to the low MHz operation of the inverters. No significant capacitive coupling was observed across the narrow opening or between adjacent lines that would allow the gate to operate at higher frequencies.

In general, for wide opens occurring in gates, fault behavior differs depending on the location of the break. When opens occur that cause pairs of transistor gates to float, it is likely that one transistor conducts and the other does not leading to Stuck-At behavior [MNN88][FTL90]. This is also supported by the research work of Henderson et al. [HSH91]. In the case where only one transistor of the gate is floating, the defective transistor is likely to be Stuck-On but the gate may function properly and switch at slower speeds. A floating transistor gate may also be susceptible to the coupling capacitances of adjacent metal conductors [RMSCR91]. However, whether or not the logic function is disturbed depends, like bridging faults, on the transistor width and length ratios, the topology of the circuit and the manufacturing process variations. Of course, independent of where the break occurs, the situation is complicated when the width of the break is narrow enough to permit electron tunneling or when the effects of leakage current dominate the effects of parasitic capacitances.

Source and drain opens exhibit different fault behavior [MB91]. Drain opens faults are optimistically characterized as non-classical. However, resistive opens present special problems since switching can occur at slower rates. These faults are best tested as slow-to-rise and slow-to-fall delay faults. Two or three cycle tests may be required in these situations to overcome timing hazards and the effects of charge sharing. Source opens can also be influenced by leakage currents leading to non-SSF behavior.

Soden and Hawkins [SH89] conclude that open defects are inherently difficult to diagnose using Stuck-At test sets, Stuck-Open test sets or $I_{DDQ}$ test sets alone. The best strategy would be to use Stuck-Open test patterns or 100 percent fault coverage Stuck-At test patterns while monitoring the current supply ($I_{DDQ}$) for each pattern as it is applied. In addition, conservative layout techniques should be used. Henderson et al. [HSH91] conclude that the best detection method for electromigration open defects is a delay test while an $I_{DDQ}$ test is suggested as a test for any kind of open with wait times of 1 second between input vectors.

### 2.3 Parametric Test

When considering all types of CMOS defects, Ferguson et al. [FTL90] state that SSF testing catches most CMOS defects but logic testing in general can miss a significant portion of the defects described above. The primary weakness of most logic testing fault models is that it applies a digital test to identify what is basically an analog defect [McE91]. CMOS defect mechanisms including GOS defects, bridging defects, open defects, transistor Stuck-On defects, punch-through defects, parasitic device defects, pn junction leakage defects and excessive contact resistance defects may not manifest as logic faults [MJ91]. The observation that most, if not all, CMOS faults can be modeled as parametric faults has caused the emergence of parametric test strategies to address the problems associated with logic-based methods.

![Figure 8. Capacitance coupled metal line and floating bridge 3 stage inverter [RMSCR91].](image-url)
There are many types of parametric tests that have been proposed [DJRX90][HM93]. Recent research interest has focused primarily on three types; \( I_{DDQ} \) [SM91], \( I_{DD} \) [FM87], and delay fault testing [HRVD77][Lin87]. \( I_{DDQ} \) is the current that flows in a circuit when all nodes have stabilized [McE91]. Given the right circuit state, the presence of a defect may cause a measurable elevation in the quiescent current by creating a conducting path between the supply rails [MJ91]. Therefore, fault observation is significantly improved since the method removes the constraint of having to propagate the fault to an observation point. \( I_{DDQ} \) has been shown to be an effective diagnostic technique for CMOS bridging defects but is of limited applicability for some types of CMOS open defects [SRW95]. Also, \( I_{DDQ} \) is handicapped by the maximum rate at which the test vectors can be applied since the current measurement can not be made until all circuit nodes have stabilized. Other problems concern the size and class of circuits that are \( I_{DDQ} \) testable. Larger circuits reduce the threshold margin between the defect-free and the defective circuit and design styles are limited to circuit structures that do not conduct current in steady-state.

Several \( I_{DD} \) approaches have been proposed to overcome the limitations of the \( I_{DDQ} \) test. For the same reasons as those presented for \( I_{DDQ} \), Frenzel and Marinos [FM87] proposed the use of the power supply as an observation point. However, they examined the dynamic behavior of the supply current as sinusoidal waveforms were applied to the primary inputs at different frequencies. Their experiments were conducted on TTL NAND gates and the power supply current was sampled to yield a power supply current signature. Defect detection decisions were based on using the mean value of the current signature as a threshold and recording the time and direction of zero crossings of the transient across the mean value.

Hashizume, et. al. [HYTK88] proposed a method which samples the \( I_{DD} \) waveform as randomly selected test vectors are applied to the circuit under test. The frequency spectrum of these waveforms are then analyzed and pattern recognition techniques are applied to identify defective devices.

Beasley et. al.[BRRAD93a][BRRAD93b] proposed a parametric test technique called \( I_{DD} \) pulse response testing. In their experiments, they biased the power and ground supply rails and the inputs at the mid-point between the low and high supply voltages and applied a pulse simultaneously to both the power and ground rails. The power rail was pulsed to \( V_{DD} \) while the ground rail was pulsed to 0 Volts. The transient current behavior was recorded for a small time interval following the delivery of the pulses. Post signal processing involved subtraction of the experimental transient waveform from a defect-free transient waveform obtained from simulations or defect-free reference chips. The resulting waveform pattern was then classified by a Feedforward Neural Network (FFNs).

Lin, et. al. [LTW+90][WLTM91] further promote the use of FFNs as a diagnostic decision tool for fault detection in analog integrated circuits. A series of experiments were conducted on analog circuits with parametric defects modeled as transistor parameter modifications including changes to junction depth, threshold voltage and oxide thickness. Both the transient and frequency response of the circuits were used as input data for the diagnostic decision algorithms.

Thibeault [Thi95] proposed a defect detection method that eliminates the need for pattern recognition by using the first harmonic to estimate the frequency spectrum of the current waveform (and output voltage waveforms).

Makki, et. al. [MSN95] proposed an \( I_{DD} \) test that compares the magnitude of the current pulse with that of a known good value. However, in order to detect the absence of a current pulse, which occurs for some open defects, test circuitry is added to allow gates to be isolated and tested in pseudo-partitions through an additional supply rail.

In general, these \( I_{DD} \)-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as \( I_{DDQ} \); however, circuit size and topology are still factors that affect the defect resolution of these schemes. Also, these methods do not provide a means of accounting for changes due to normal process fluctuations and are therefore subject to aliasing problems.

Alternatively, delay fault testing takes advantage of the fact that many CMOS defects cause a change in the propagation delay of signals along sensitized paths [SH89]. Unlike \( I_{DDQ} \), a delay fault test samples the logic values of the latches or primary outputs at a timed instance and compares them with a set of expected values. The threshold value in a delay fault test is time instead of current and the test is dynamic instead of static. In this respect, delay fault testing does not suffer from slow test vector application rates, like \( I_{DDQ} \), and is not sensitive to circuit size or structure as is true of \( I_{DD} \). However, since defect detection is accomplished by sampling logic states at the terminal nodes of sensitized paths, test vector generation is more complicated than it is for \( I_{DDQ} \) and...
logic testing strategies since test paths must be sensitized from a primary input (PI) to a primary output (PO) [HRVD77]. Another problem concerns invalidation due to static and dynamic hazards [PR88]. Since the primary outputs are not monitored continuously, care must be taken that sensitized paths reconvergent on gates along the tested path do not cause the outputs of the gates to transition before the tested path has propagated its transition through the gates. Lastly, since the number of possible paths is much larger than the number of paths that are actually tested, the effectiveness of a delay fault test is dependent on the propagation delay of the tested paths and the delay defect size, for path delay fault testing, and the accuracy of the test equipment, for gate delay fault testing [PMW88]. Lastly, Pierzynska and Pilarski [PP95] have shown that a non-robust test can detect a delay fault undetectable by any robust test.

More recently, Franco and McCluskey [FM91] proposed a device testing method that extends the delay fault test method by analyzing the circuit’s output response continuously instead of sampling at specific time intervals. Two techniques are suggested which can be characterized based on whether the continuous sample is taken before or after the normal sampling point. Pre-sampling refers to monitoring the output signal for the time period between the latching of the second test vector at the PIs and the normal sampling event at the POs. Post-sampling refers to monitoring the output signal for a time interval following the normal sampling event. The objective of post-sampling waveform analysis is to determine if the output signal changes state after the normal sampling event. If a delay fault occurs then at least one circuit output will be unstable at the sampling time and a change in state will be observed on the output line during the observation period. Post-sampling is more robust then standard delay fault testing since any changes during the observation period are an indication that a dynamic hazard has invalidated the delay fault test. Pre-sampling is more sensitive to small delay faults but is more difficult to implement since transitions may occur during the observation period for both the defective and defect-free circuits. One way to differentiate between these cases is to take the average value (analog integral) of the output waveform. This yields a measure of the delay and allows detection of delay faults without requiring them to be sensitized through the longest path. The hardware overhead of this method is significantly greater when compared with post-sampling waveform analysis and the output signal storage requirements also pose a problem in terms of practicality. Integration accuracy and aliasing problems are also issues that need to be addressed. Chatterjee, et. al. [CJPA96] discussed a similar output waveform integration method for the detection of stuck-at failures.

Dorey et. al. [DIRR88] evaluated a number of parametric test strategies for reliability testing of CMOS devices including \( I_{DDQ} \), transient supply current monitoring, delay fault testing, upper cut-off frequency determination (the maximum speed of operation as a function of the supply voltage), supply current low frequency noise monitoring and transient supply current noise monitoring. Simulation experiments were conducted to determine the sensitivity of device parametric properties to changes in transistor gain factors, threshold voltages and other transistor and circuit topology characteristics. Temperature and radiation stress test experiments were conducted on real devices to determine if a relationship existed between initial parametric abnormalities and early failure. They found that the current transient test provided a great deal of information about individual component integrity but required sophisticated data capture and post processing equipment in order to make an accurate defect detection decision. Sequential circuits were more well suited to the cut-off frequency test while combinational circuits were more well suited to the delay test. Both types of tests were very sensitive to changes in threshold voltage, gain factor, leakage currents and supply voltage. The supply current low frequency noise test and the transient supply current noise test were sensitive defect detection methods but both were slow tests to apply and required sophisticated data processing to improve signal-to-noise ratios.

Recently, Ma, et. al. [MFM95] and others [HSRF94][SH89][MAH92][HSF91] evaluated a large number of test methodologies and determined that a combination of several test strategies may be necessary in order to find all defective devices. In particular, Ma, et. al. discovered that \( I_{DDQ} \) cannot detect all kinds of defects and must be used with some kind of dynamic voltage test. Our technique, Transient Signal Analysis (TSA), with its advantages in defect detection and process insensitivity, is proposed as an addition to this test suite.

### 2.4 Transient Signal Analysis (TSA)

TSA is based on a measurement of the contribution to the transient response of a device by physical characteristics such as substrate, power supply or parasitic coupling which are present in any circuit. In this paper, we demonstrate through simulation experiments that global variations of major device performance parameters, i.e. threshold voltage and gate...
oxide thickness, result in measurable changes of the circuit’s transient response at all test points. In contrast, the presence of a device defect will change both the value and topology of the parasitic components in the region of the defect. For example, a single open circuit for the connection to the drain terminal of a CMOS transistor will remove a percentage of the normal parasitic capacitance present on the output node of the associated logic gate. Similarly, a bridging short between two or more gate output lines will add new parasitic resistive and capacitive elements at each of the shorted nodes. We present other simulations experiments that demonstrate that the changes introduced by defects result in measurable variations in the transient response and that these variations are distinct at two or more test points.

By analyzing the transients at multiple test points and assuming process variation is uniform across individual die, TSA is able to distinguish between the changes in the transient response caused by defects and those caused by process variation. This is true because, in the latter case, the transients generated at each of the test points will be correlated in the defect-free device. On the other hand, the presence of a defect will have a larger influence on the transients at test points closer to the defect. Therefore, defect detection is accomplished in TSA by analyzing the transients at all test points simultaneously so that global process variations can be distinguished from the regional defect variations.

3.0 Experimental Circuit

In this section, we will present the details of the procedure followed to produce the simulation results. The digital design chosen for study in this paper is the ISCAS85 c432 benchmark circuit. A schematic diagram of the c432 is shown Figure 9. The ITD/AµE (Advanced Microelectronics Division) scmos standard-cell library was used in the synthesis of the c432.

The schematic diagram shown in Figure 9 has labels and arrows indicating the areas where modifications were made both to suit the synthesis software and to enhance performance characteristics. Three nine-input AND gates are used in the original ISCAS85 specification at the locations shown by the arrows in Figure 9. Due to the poor performance characteristics of this gate, no standard cell exists for it in the ITD/AµE library. Consequently, the nine-input AND gates used in the specification were replaced by the equivalent circuit shown in Figure 10.

In addition, cascaded inverters are used to enhance the current driving capabilities of large fan-out points also indicated in Figure 9. The ISCAS85 netlist description of the c432 specifies that each of the three 9-input AND gates drive a single inverter. The inverter is then responsible for driving a fan-out of nine. However, after analyzing an OCTOOL’s generated standard-cell implementation of the circuit using SPICE, switching at these fan-out points was dominating the timing.

Figure 11 shows the steps taken in the synthesis and extraction of c432. Figure 12 shows a block-level diagram of the layout created for the simulation experiments. The cells labeled SCN08-in and invf104 identify modifications that were made to the MAGIC layout before the extraction was performed. The test stimulus used in the simulation experiments switch PI 17IN with the other 35 PIs held low. This stimulus toggles all primary outputs in addition to exercising all five of the largest fan-out stems shown in Figure 9. Consequently, only one input pad was added to the layout. The output signal of the SCN08-in pad is re-inverted to provide a reference signal to the input of the core logic. Figure 12 also shows the test points monitored in the experiments. The output lines of the gates driving the seven POs were monitored directly and the output pads have been omitted for this simulation work. The current transients generated by the internal gates on the power supply terminal were also monitored. The current transients generated by the switching of the input pad were separated from those generated by the core logic as indicated in the figure.

The Hewlett-Packard (HP) CMOS26B process data sheets from MOSIS run n33h were used in the simulations since both the SPICE transistor models and the MAGIC extraction parameters were available for this run. HP’s CMOS26B process line is a 1.0µm feature size process. The extraction was performed using the MAGIC extract procedure.

4.0 Results

The objective of the simulation experiments is four fold. First, we determine the effects that normal process variation will have on the transient response of the c432. Second, we show that the changes in transient behavior caused by defects occurring on off-sensitized paths can be observable at the test points. Third, we show that the observation of the defect is possible in the presence of normal process variation. Fourth, we determine the high speed frequency response of the input/output pads and the effects that the pads will have on the introduction and observation of the circuit’s transient response.

4.1 Raw Waveform, Post-Processings and Normal Process Variation

The results of the simulation experiments con-
Figure 9. Schematic diagram of ISCAS85 c432 with gate driver modifications.

9-input AND gate broken down into equivalent gate structure

Extra inverters inserted to improve circuit performance

223OUT
329OUT
370OUT

421OUT
430OUT
431OUT
432OUT
Figure 10. 9-input AND gate equivalent circuit used in the OCTTOOL's synthesis of the c432.

Figure 11. Block-level diagram showing the method and the software tools used in the synthesis, extraction and simulation of the c432.

Figure 12. Block diagram of experimental model (not drawn to scale).
ducted on the c432 in the absence of defects are presented in this section. Section 4.1.1 describes the test point signals and shows examples of raw waveforms. Section 4.1.2 discusses the post-processing steps performed on the raw waveforms. Section 4.1.3 examines normal process variation.

4.1.1 Raw waveforms

Figure 13 shows the results of a SPICE simulation experiment conducted on the c432 using a nominal set of SPICE modeling parameters. The waveform labeled 17INpad is the controlling SPICE input waveform applied to the input pad. 17IN identifies the post-pad (buffered) waveform generated on PI line 17 of the c432. The seven test point waveforms are labeled as 223OUT, 329OUT, 370OUT, 421OUT, 430OUT, 431OUT and 432OUT in the figure. Figure 13 also shows the current behavior through the SPICE source suppling the V_DD terminal of the c432.

Figure 14 shows the raw waveforms of the c432 when the Gate Oxide thickness of all transistors is reduced by 10 percent. Since the changes in the shape of the waveforms shown in Figures 13 and 14 are difficult observe using the raw waveforms directly, a post-processing step is performed.

4.1.2 Waveform Post-Processing Procedure

Each of the raw waveforms have been post-processed so that changes in the transient behavior caused by defects and process variations are amplified with respect to the large (logic) signal behavior. The post-processing involves subtracting the raw waveforms produced by the introduction of process variation or defects from a standard set of raw waveforms. The raw waveforms shown in Figure 13 represent the nominal device and have been used as the standards for the experimental results shown in this paper.

Figure 15 shows an example of the post-processing procedure. The difference waveform that results from the subtraction of the Standard raw waveform and Defective raw waveform is shown shaded in black in the figure. The polarity of the changes in transient behavior above and below the baseline are captured using this technique and can be used as additional discriminatory information. The post-processed difference waveforms will be referred to as Signature Waveforms (SWs) hereafter.

4.1.3 Normal Process Variation

Normal process variation occurs unavoidably within the fabrication process. Changes in fabrication process parameters alter the performance characteris-
tics of devices in ways that are difficult or impossible to model analytically [Str82]. These natural fluctuations result in changes in device circuit parameters such as capacitance and resistance of interconnect and transistor device parameters. Dorey et al. [DJRX90] have identified two major performance determining circuit parameters, both of which are affected by process variation as threshold voltage and gate oxide thickness. The normal tolerances of these circuit parameters are difficult to define because of the non-linear relationship between them and the performance characteristics of the device. ICs that are fabricated above or below the tolerances may have undesirable electrical characteristics and consequently fail performance specifications. These ICs will be considered defective in our testing method even though the defect is a parametric defect and not a catastrophic defect. The performance specification will dictate how much fluctuation in these and other circuit parameters is permissible. The simulation results presented below show the effects on the c432’s transient response when these parameters are varied globally by 5 and 10 percent above and below their nominal values. Other simulation experiment results

Figure 15. Example of a standard raw waveform, a defective raw waveform and a Signature Waveform.

Figure 16. SWs generated using a 5% increase in Gate Oxide thickness for all transistors.

Figure 17. SWs generated using a 10% increase in Gate Oxide thickness for all transistors.
will be presented in Section 4.2.6 that show the changes in transient response when these circuit parameters are modified by plus and minus 25 percent.

Figures 16 and 17 show the SWs of the POs and VDD terminal resulting when the Gate Oxide thickness (TOX in the SPICE transistor model) is increased by 5 and 10 percent. The patterns are primarily a result of changes to the transistor gain factors which cause changes in the propagation delays of signal paths. Increasing the Gate Oxide thickness reduces the gain and increases the propagation delay. Both sets of SWs have similar shapes characterized primarily by differences in magnitude.

Figures 18 and 19 show the set of SWs that result when the Gate Oxide thickness of every transistor is reduced by 5 and 10 percent. Again, a similarity exists among the sets of SWs in terms of shape. However, the global effect on transistor performances is not as severe when compared with the corresponding SWs resulting from an increase in Gate Oxide thickness.

Figures 20 through 23 show the SWs resulting when the Threshold Voltage is increased and decreased by 5 and 10 percent. The SW shapes are sharper than those resulting from increases in Gate Oxide thickness. A strong linearly is observable...
between the four sets of SWs. Also unlike the relationship between increases and decreases in Gate Oxide thickness, a symmetrical relationship exists for corresponding changes in Threshold Voltage above and below the nominal value.

The main challenge of using this device testing technique concerns the visibility of defects in the presence of normal process variation. The sets of SWs resulting from changes in Gate Oxide thickness and Threshold Voltage are significant. The tolerances defined by the IC specification will determine whether the classification of 10 percent variance is normal or abnormal.

4.2 Defective Device Transient Behavior

4.2.1 Resistive Bridging Defect

The first defect we will examine is a bridging defect. A bridge has been introduced as a resistive short between the output of a norf201 standard-cell NOR gate and the output of an xorf201 standard-cell XOR gate. The lines affected are labeled as 199 and 333 in the schematic diagram shown in Figure 9. A segment of the schematic is shown in Figure 24. In the non-defective circuit, transitions on line 333 occur after transitions on line 199 due to the additional gate delays on sensitized paths to the XOR gate that drives
The consequences of a bridging short were examined in section 2.0 and an analogous situation is shown in Figure 3. The test sequence described above will not cause a logic fault to occur since both of the shorted lines are initialized to logic 1 by the first vector and both transition to logic 0 for the second vector. In order for this type of defect to cause a logical fault, three conditions must be satisfied: one of the test vectors must set the state of the shorted lines to opposite potentials, the current-drive capability of one of the gates must dominate the other and a sensitized path must be generated by the test vector from the weaker node to a PO so the fault can be observed. Since the first condition is not satisfied, the other conditions are irrelevant.

$I_{DDQ}$ can not be used reliability as a detection strategy since no contention exists between the shorted nodes in steady-state. The best chance of detecting the defect using this test sequence is through the use of a small delay-fault test. As a consequence of the short, the normal propagation delay at line 333 is reduced since the transition of line 199 to logic 0 creates a voltage drop across the short and causes the voltage at line 333 to drop prematurely.

4.2.1.1 100 Kilo Ohm Resistive Bridge

The importance that the resistance of a short has on the fault behavior observable has been examined in section 2.0. We have modeled the short between lines 199 and 333 at three different resistances, 100 Kilo Ohms, 4 Kilo Ohms and 500 Ohms, in order to evaluate the changes that resistance will have on the shape of the SW. Figure 25 shows the SWs with the short modeled at 100 Kilo Ohms. The magnitudes of the voltage transients are small (~300 MilliVolts) but still observable.

4.2.1.2 4 Kilo Ohm Resistive Bridge

Figure 26 shows the SWs that result when the short is modeled at 4 Kilo Ohms. The effect of the short has a dramatic effect on the output lines whose transitions are a direct consequence of lines sensitized from the short. However, differences due to propagation delay alone may not be a clear indicator that a defect exists since propagation delays are also observed in the SWs of simulation runs modeling the effects of process variation. However, process variation usually affects the transient behavior of the IC as a whole causing similar behavior at all sampling points. Changes in the transient behavior due to a defect are regional in Figures 25, 26 and 27 supporting our hypothesis that multiple sampling points are nec-
necessary in order to distinguish between these cases. The IDD SW captures the temporal variations that result from the change in propagation delay along the paths to POs 223OUT, 329OUT and 370OUT. However, this single SW can not be used alone to identify the defective device for the same reason that a single voltage test point can not be used. This output used in conjunction with the voltage test points provides a strong indication that the variation is regional and that it is due to the presence of a defect.

### 4.2.1.3 500 Ohm Resistive Bridge

Figure 27 shows the SWs that results when the short is modeled at 500 Ohms. The change in transient behavior of POs 223OUT, 329OUT and 370OUT clearly indicates the presence of the defect. The same is true for the current SW through the VDD terminal.

### 4.2.2 Stuck-Open Fault

An example of a defect that is difficult to detect using any existing testing method is shown in Figure 28. The shaded resistor identifies the defect injection point in the NOR gate. The non-classical Stuck-Open defect is modeled with a resistance of 1 Mega Ohm. In this experiment, the path on which the Stuck-Open defect is modeled is not exercised. The test vector sequence toggles line 17IN from 0 to 1 and then back to 0 as shown in italic next to the label in the figure. The first vector sets line 183 to 0 Volts through transistor N1 and the second vector sets line 183 to VDD through transistors P1 and P2. The third vector restores the original state of the NOR gate.

Figure 29 shows the SWs resulting from a 1 Mega Ohm Stuck-Open defect. PO 329OUT most clearly shows the effect that the defect has on the transient response of the c432. PO 370OUT is also effected slightly. The IDD transient also indicates that a defect exists. This defect will also be examined in the presence of normal process variation in Section 4.3.

### 4.2.3 Redundancy Fault

Figure 30 shows a schematic diagram of the invf104 standard cell used in the synthesis of the c432. The gate is redundant since the four parallel inverters
all drive the output line 309. No logic fault results from this defect. Parametric testing strategies must be used in order to detect these types of defects. The test vector used to generate the SWs switch this gate on a sensitized path to PO 370OUT.

The SW for PO 370OUT in Figure 31 shows the effect of the defect most clearly. Since a p-channel transistor has been effectively removed by the defect, the current drive capability of this gate is reduced causing an increase in propagation delay along paths driven by the gate. The current SW is also influenced by the defect. Used in conjunction with PO 370OUT.
and the other POs, the defect can be detected due to the regional variation that occurs.

4.2.4 Charge Sharing

Figure 32 shows the schematic diagram of the xorf201 standard cell used in the synthesis of the c432. The experiment was originally designed to illustrate the effects of charge sharing.

Figure 31. SWs resulting with a 1 Mega Ohm open drain defect in a 4X INVERTER with redundancy.

Figure 32. Open drain in the xorf201 standard cell originally designed to illustrate the effects of charge sharing.

Figure 33. SWs resulting from a SPICE simulation run with a 1 Mega Ohm open drain of a XOR gate.

and the other POs, the defect can be detected due to the regional variation that occurs.

the effect of charge sharing and the problems it creates for logic test. However, due to the differences signal arrival times on lines 203 and 159, the output line, 227, was discharged to ground through the left pair of series n-channel transistors shown on the bottom right of Figure 32. The SWs shown in Figure 33 illustrate the logic error on POs 329OUT and 370OUT that
4.2.5 Stuck-At Fault

Figure 34 shows an experiment designed to examine the transient behavior resulting from a Stuck-At defect present on the gate line of a 4-input NAND gate. Gate input 246 is not exercised and remains high during the test vector sequence. Figure 35 shows the resulting SWs. The change in transient behavior is small but measurable at a subset of the POs of the c432.

4.2.6 Abnormal Process Variation

The sets of SWs resulting from 25 percent changes in Gate Oxide thickness and Threshold Voltage have magnitudes that extend across the entire range of voltages possible. Figures 36 and 37 show the SWs resulting when the Gate Oxide thickness (TOX in the SPICE transistor model) is changed by 25 percent above and below the nominal value. Since these changes caused the propagation delays to increase by as much as 1.5 nanoseconds, we have classified these devices as defective.

Figures 38 and 39 show the effects on the transient response when the Threshold Voltage is changed by 25 percent above and below the nominal value. These devices are also classified as defective.

4.3 Defects in the Presence of Process Variation

The ability to recognize defect transient behavior in the presence of variations caused by changes in process parameters is essential to the accurate classification of defective and defect-free devices. This section shows several experimental results in which SPICE transistor parameters are modified to model process variation in the presence of a defect.

Figure 40 shows the resulting SWs when the defect shown in Figure 30 is inserted into the c432 and Gate Oxide thickness is increased globally by 5 percent. Figure 40 shows a magnified region of PO 370OUT illustrating that the changes in transient response are additive and the defect SW is superimposed on the SW resulting from process variation. A similar conclusion can be made between the $I_{DD}$ SWs also shown in Figure 40.

Figure 42 shows the SWs resulting from the presence of the Stuck-Open defect shown in Figure 28 and a 5 percent increase in Threshold Voltage. The SW of PO 329OUT indicates that the defect can be detected.
By comparing the SWs of this PO in Figures 20 and 42, the transient on the right portion of the waveform is clearly reduced in magnitude. The $I_{DD}$ SWs from these figures also show a change in this region of the waveform.

### 4.4 I/O Pad Analysis

A frequency response analysis of the input/output pads will determine the high frequency attenuation of the circuit's transient response. The bandwidth limitations of the pads will bound the range of frequencies that can be introduced at the primary inputs and those that can be observed at the primary outputs. This section will present the results of simulation experiments conducted on several selected pads from two different technologies.

Figures 43 and 45 show SPICE simulation results comparing the transition edges of two pad sets, the SCN20-IO bi-directional pad used with 2 µm processes and the SCN08-in and SCN08-out used with a 1 µm processes. Figure 43 shows the simulation results of the SCN08-in pad and SCN20-IO pad configured as
an input pad while Figure 45 shows the simulation results of the SCN08-out pad and the SCN20-IO pad configured as an output pad. Since the SCN08-in pad inverts the signal applied to the pad terminal, the in complement terminal of the SCN20-IO is used for the comparison. An invf101 inverter is added to the lay-
out as a load device when the pads are simulated as input pads. The published package pin resistance and capacitance is added to the SPICE file as the load when the pads are simulated as output pads. The extraction parameters used for the three MAGIC extractions are those published by MOSIS (MOS Implementation Systems) from actual wafer test structures. The matching SPICE transistor model parameters derived by MOSIS from the same wafers are also used for the simulation runs. The difference in rise and fall time behavior between the two pad sets results from both scaling and the use of simpler designs for the 1.0\(\mu\)m process SCN08 pads.

The SPICE source waveform specification includes a 5 nanosecond delay followed by a 10 nanosecond pulse. The period of the pulse is 20 nanoseconds and the rise-time and fall-time of the edges are specified at 0.5 nanoseconds. It is recognized that these edges would be difficult to achieve in actual testing environments but they serve to illustrate the response of the pads under ideal conditions. Figure 43 shows the inverted waveforms for the SCN08-in pad and the SCN20-IO pad configured as an input pad. The rise and fall times of the SCN08-in pad are almost identical at 0.2 nanoseconds. However, the rise and fall times of the SCN20-IO pad are 1.8 and 1.6 nanoseconds respectively. Figure 45 shows the waveforms when the pads are configured as output pads. In both cases, the response times are much worse with rise and fall times at 1.5 and 4.5 nanoseconds for the SCN08-out pad and the SCN20-IO pad, respectively.

Another experiment illustrates that the change in resistance and capacitance of the interconnect due to a feature size change only is not a linear function. For example, when the SCN20-IO pad is extracted using \(\lambda = 0.5\), the average resistance of the pad’s interconnect is reduced by 93.5 percent when compared with the \(\lambda = 1.0\) extraction. Additionally, average substrate
capacitance is reduced by 77.5 percent. However, average internodal coupling capacitance increases by 476 percent when the feature size is cut in half. This serves to illustrate that crosstalk between disjoint circuit nodes will become more evident as devices are scaled down. The increase in crosstalk will permit signal variation produced by a defect to be more easily measured on off-sensitized nodes further increasing defect visibility.

SPICE provides the ability to perform a fourier analysis on the waveforms generated from a simulation experiment. A fourier analysis of the waveforms shown in Figures 43 and 45 is shown in Figures 44 and 46. Only the first nine harmonics of original waveforms are shown. The magnitudes of the individual frequency components for the input signal and for each of the output signals of the SCN08-in and SCN20-IO are shown from left to right, respectively, for each frequency in the bar graph. The frequency spectrum for the SPICE source and SCN08-in output signals are nearly identical and the SCN20-IO spectrum illustrates only moderate attenuation in the pad.
of the higher frequency components of the source signal.

Figure 46 illustrates the more significant attenuation that occurs when the pad is configured as an output pad. In this case, the higher frequencies have essentially been eliminated for the SCN20-IO pad and moderately attenuated for the SCN08-out pad. If the filtering effects of the output pads are significant enough to remove the important features of the output signals, then the insertion of specific test points on the interior of IC will be necessary to allow sampling that bypasses the circuitry of the pad. The transmission capabilities of the pads will need further evaluation when a means to obtain a more accurate device model is available.

The padframe also contains a set of unbuffered pads dedicated to supplying power and ground to the internal circuit. Since the power and ground pads are not buffered, they do not exhibit the filtering behavior observed in the SCN20-IO pads. Consequently, they provide ideal signal injection points or observation points. Another advantage in using the power and ground supply pads as sampling points is that their presence is guaranteed and free in terms of design cost and integration.

5.0 Summary and Conclusions

A parametric device testing method has been proposed in this paper called Transient Signal Analysis (TSA). The method uses the voltage transients as well as the current transients generated within the IC as a defect detection mechanism. The difference waveforms produced by subtracting the transient signals generated by test ICs from the transient signals generated by reference ICs are called Signature Waveforms (SW). The SWs capture the changes in the IC’s transient response resulting from the presence of one or more defects or from variations occurring in process parameters.

The simulation results of the c432 presented in this proposal indicate that defects affect the transient response of the circuit and that the observance of this change is possible without having to explicitly exercise the path disrupted by the defect. We have shown that the presence of a defect will change the values of the parasitic components in the region of the defect. If the altered parasitics are adjacent to sensitized paths that are exercised with the sequence of test vectors, then the transient behavior of the signal is also altered and propagated to the primary outputs of the IC. By analyzing the transients at multiple test points and assuming process variation is uniform across individual die, TSA is able to distinguish between the changes in the transient response caused by defects and those caused by process variation. This is true because, in the latter case, the transients generated at
each of the test points will be correlated in the defect-free device. On the other hand, the presence of a defect will have a larger influence on the transients at test points closer to the defect. The results of simulation experiments have shown that defects cause variations in only a subset of the test point signals while changes in process/circuit parameters cause variations to occur proportionally in all test point signals. Therefore, defect detection is accomplished in TSA by analyzing the transients at all test points simultaneously so that global process variations can be distinguished from the regional defect variations.

TSA testing offers advantages over existing device testing techniques such as Stuck-At testing, $I_{DDQ}$ testing and Delay Fault testing. In the introduction we noted that logic testing methods are characterized by a requirement for large sets of test vectors in order to achieve adequate fault coverage. Parametric testing methods like $I_{DDQ}$ are limited by the application rate of the test vectors which can significantly extend the production line test in addition to having problems with sensitivity for large circuits. Delay fault testing is more sensitive. However, test vector generation is complicated by the requirement for sequences of test vectors. $I_{DD}$ pulse response testing is based entirely on the transient activity of the current in the power and ground rail and in this way is similar to the technique that we are proposing. However, the resolution achievable using this single signal source is bounded by the number of circuit components that are directly connected to it. In addition, circuit components like transmission gates are isolated from the power and ground supply rails further reducing the visibility of defects that occur within these components.

Because TSA is capable of measuring variations in transient signals on off-sensitized paths, the number of test vectors required may be smaller when compared with other parametric techniques. Moreover, there are no constraints on the types of topologies that can be tested using TSA testing. TSA testing also captures the delay characteristics of signal propagation paths without requiring the accurate timing of test vectors and sampling periods. Furthermore, test vector sequences are not invalidated due to the presence of static and dynamic hazards as they are in delay fault testing. TSA testing also utilizes selected test signal sampling points providing better resolution and therefore better defect observability when compared with the $I_{DD}$ pulse response testing method.

References


