OBSOLETE

MICRON TECHNOLOGY, INC.

4, 8 MEG x 36 PARITY DRAM SIMMs

DRAM MODULE

MT12D436
MT24D836

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single in-line memory module (SIMM)
- 16MB (4 Meg x 36) and 32MB (8 Meg x 36) parity versions
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) access cycle
- Multiple RAS# lines allow x18 or x36 widths

OPTIONS — MARKING

- Timing
  - 60ns access — -6
- Packages
  - 72-pin SIMM — M
  - 72-pin SIMM (gold) — G
  - 72-pin SIMM low profile (1.00") — DM
  - 72-pin SIMM (gold) low profile (1.00") — DG

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

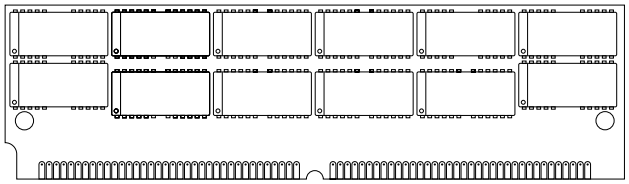
PART NUMBERS

PART NUMBER	CONFIGURATION	PLATING	HEIGHT
MT12D436G-xx	4 Meg x 36	Gold	1.190"
MT12D436M-xx	4 Meg x 36	Tin/Lead	1.190"
MT12D436DG-xx	4 Meg x 36	Gold	1.000"
MT12D436DM-xx	4 Meg x 36	Tin/Lead	1.000"
MT24D836G-xx	8 Meg x 36	Gold	1.190"
MT24D836M-xx	8 Meg x 36	Tin/Lead	1.190"

xx = speed

PIN ASSIGNMENT (Front View)

72-Pin SIMM
(DD-5) 4 Meg x 36 (shown)
(DD-6) 8 Meg x 36
(DD-7) 4 Meg x 36 Low Profile



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	Vss	57	DQ14
4	DQ2	22	DQ6	40	CAS0#	58	DQ32
5	DQ20	23	DQ24	41	CAS2#	59	Vcc
6	DQ3	24	DQ7	42	CAS3#	60	DQ33
7	DQ21	25	DQ25	43	CAS1#	61	DQ15
8	DQ4	26	DQ8	44	RAS0#	62	DQ34
9	DQ22	27	DQ26	45	NC/RAS1#*	63	DQ16
10	Vcc	28	A7	46	NC	64	DQ35
11	NC	29	NC (A11)	47	WE#	65	DQ17
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC/RAS3#*	51	DQ11	69	PRD3
16	A4	34	RAS2#	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	Vss

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The MT12D436 and MT24D836 are randomly accessed 16MB and 32MB solid-state memories organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS# is used to latch the first 11 bits and CAS# the latter 11 bits. A READ or WRITE cycle is selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS#. Since WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

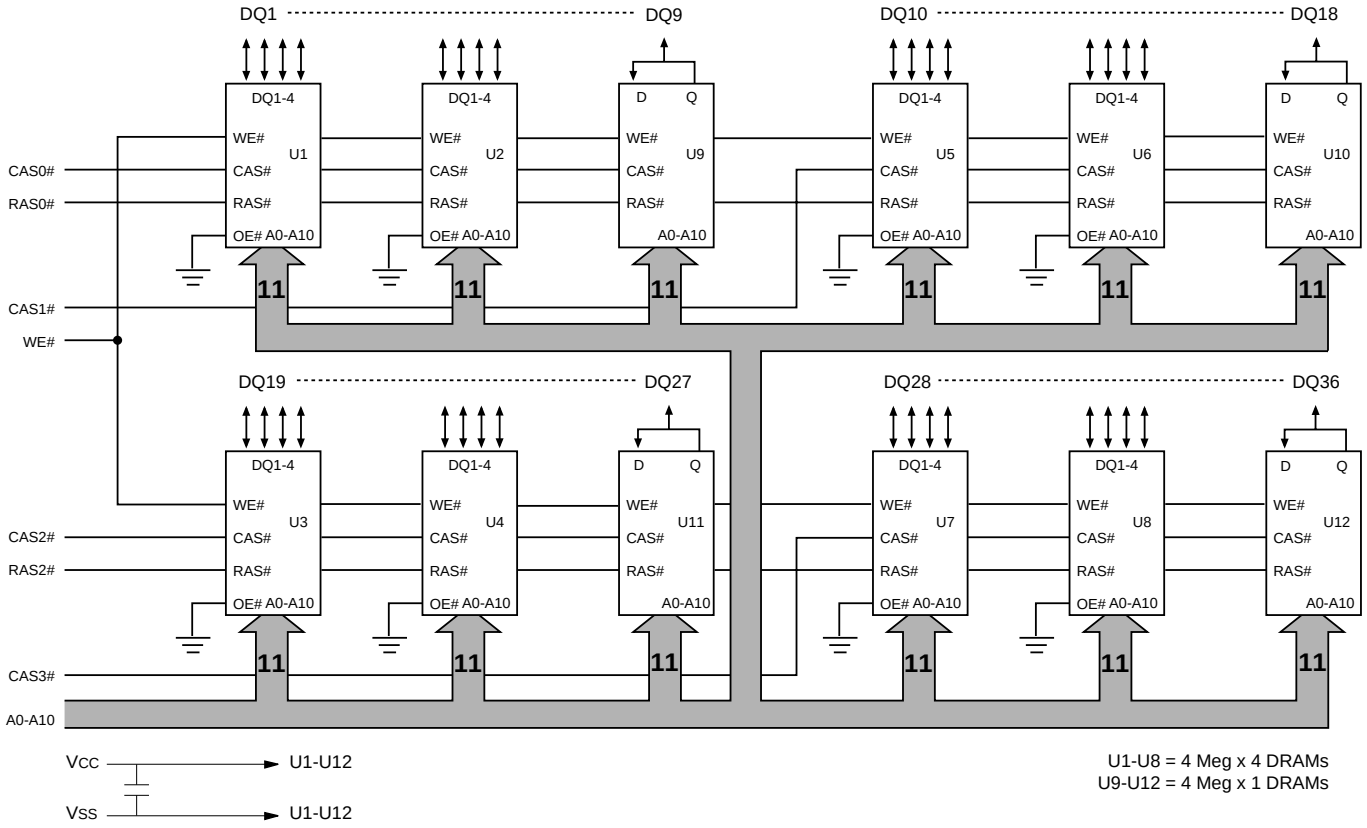
REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS# addressing.

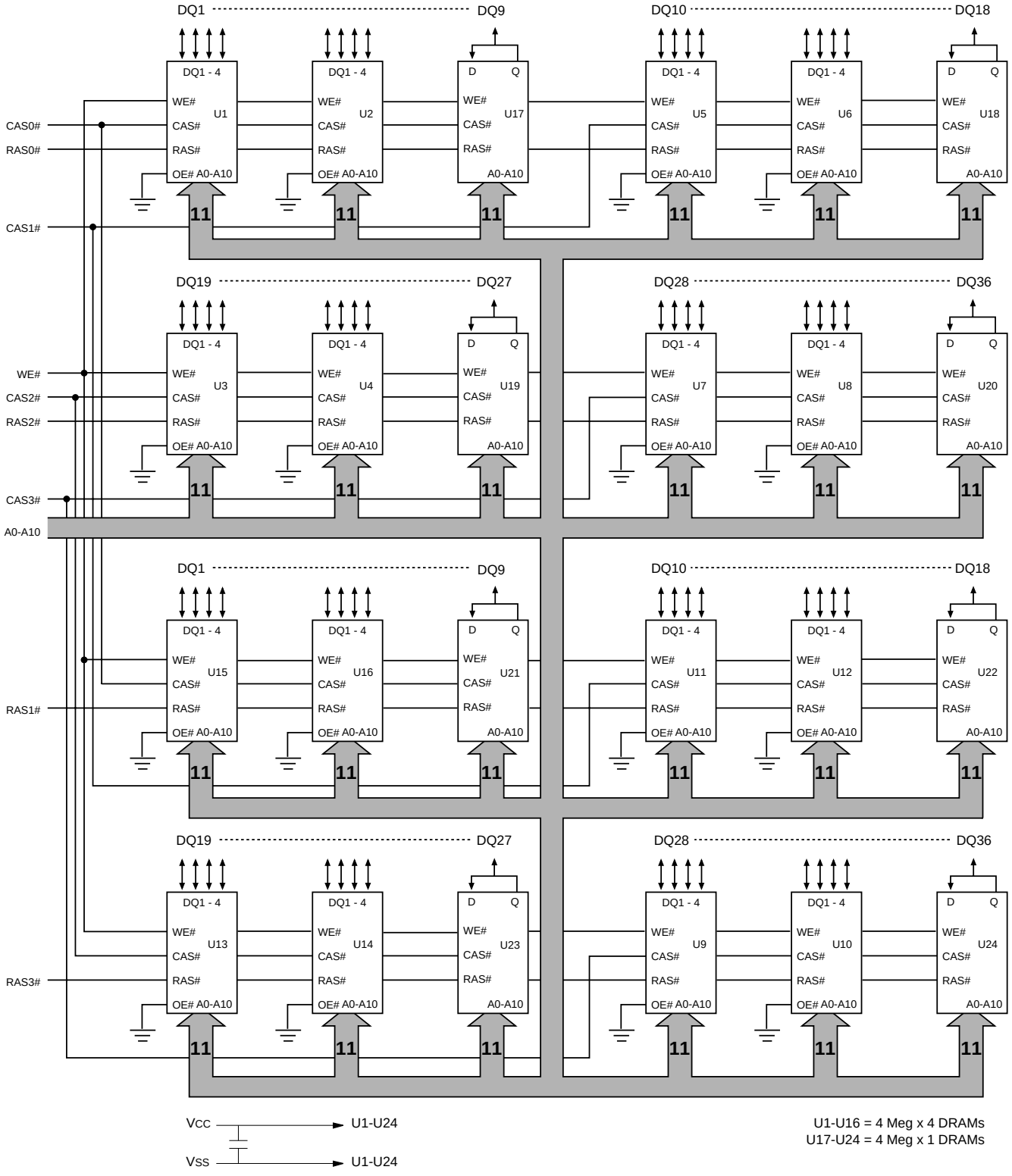
x18 CONFIGURATION

For x18 applications, the corresponding DQ and CAS# pins must be connected together (DQ1 to DQ19, DQ2 to DQ20 and so forth, and CAS0# to CAS2# and CAS1# to CAS3#). Each RAS# is then a bank select for the x18 memory organization.

FUNCTIONAL BLOCK DIAGRAM
MT12D436 (16MB)



FUNCTIONAL BLOCK DIAGRAM
MT24D836 (32MB)



U1-U16 = 4 Meg x 4 DRAMs
U17-U24 = 4 Meg x 1 DRAMs

TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	ADDRESSES		DATA-IN/OUT
					^tR	^tC	DQ1-DQ36
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS#-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

JEDEC-DEFINED PRESENCE-DETECT – MT12D436 (16MB)

SYMBOL	PIN	-6
PRD1	67	V_{SS}
PRD2	68	NC
PRD3	69	NC
PRD4	70	NC

JEDEC-DEFINED PRESENCE-DETECT – MT24D836 (32MB)

SYMBOL	PIN	-6
PRD1	67	NC
PRD2	68	V_{SS}
PRD3	69	NC
PRD4	70	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +125°C
Power Dissipation 12W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	5.5	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT	RAS0#-RAS3#	I_{I1}	-12	12	µA	
Any input 0V ≤ V_{IN} ≤ 5.5V	A0-A10, WE#	I_{I2}	-48	48	µA	23
(All other pins not under test = 0V)	CAS0#-CAS3#	I_{I3}	-12	12	µA	23
OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ36	I_{OZ}	-10	10	µA	23
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	16MB 32MB	22 44	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = other inputs = V_{CC} -0.2V)	I_{CC2}	16MB 32MB	16 32	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	16MB 32MB	1,400 1,422	mA	3, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	16MB 32MB	1,040 1,062	mA	3, 22
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	16MB 32MB	1,400 1,422	mA	3, 22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	16MB 32MB	1,400 1,422	mA	3, 4

CAPACITANCE

		MAX			
PARAMETER	SYMBOL	16MB	32MB	UNITS	NOTES
Input Capacitance: A0-A10	C_{I1}	70	140	pF	2
Input Capacitance: WE#	C_{I2}	94	188	pF	2
Input Capacitance: RAS0#, RAS1#, RAS2#, RAS3#	C_{I3}	50	50	pF	2
Input Capacitance: CAS0#, CAS1#, CAS2#, CAS3#	C_{I4}	25	50	pF	2
Input/Output Capacitance: DQ1-DQ8, DQ10-DQ17, DQ19-DQ26, DQ28-DQ35	C_{IO1}	10	18	pF	2
Input/Output Capacitance: DQ9, DQ18, DQ27, DQ36	C_{IO2}	16	28	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Access time from CAS#	^tCAC		15	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# hold time (CBR REFRESH)	^tCHR	15		ns	4
CAS# to output in Low-Z	^tCLZ	3		ns	21
CAS# precharge time	^tCP	10		ns	13
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	10		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR REFRESH)	^tCSR	10		ns	4
Write command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	18
Data-in setup time	^tDS	0		ns	18
Output buffer turn-off delay	^tOFF	3	15	ns	17, 21
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	15
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	20		ns	14
Read command hold time (referenced to CAS#)	^tRCH	0		ns	16
Read command setup time	^tRCS	0		ns	
Refresh period (2,048 cycles)	^tREF		32	ms	
RAS# precharge time	^tRP	40		ns	
RAS# to CAS# precharge time	^tRPC	0		ns	

AC ELECTRICAL CHARACTERISTICS

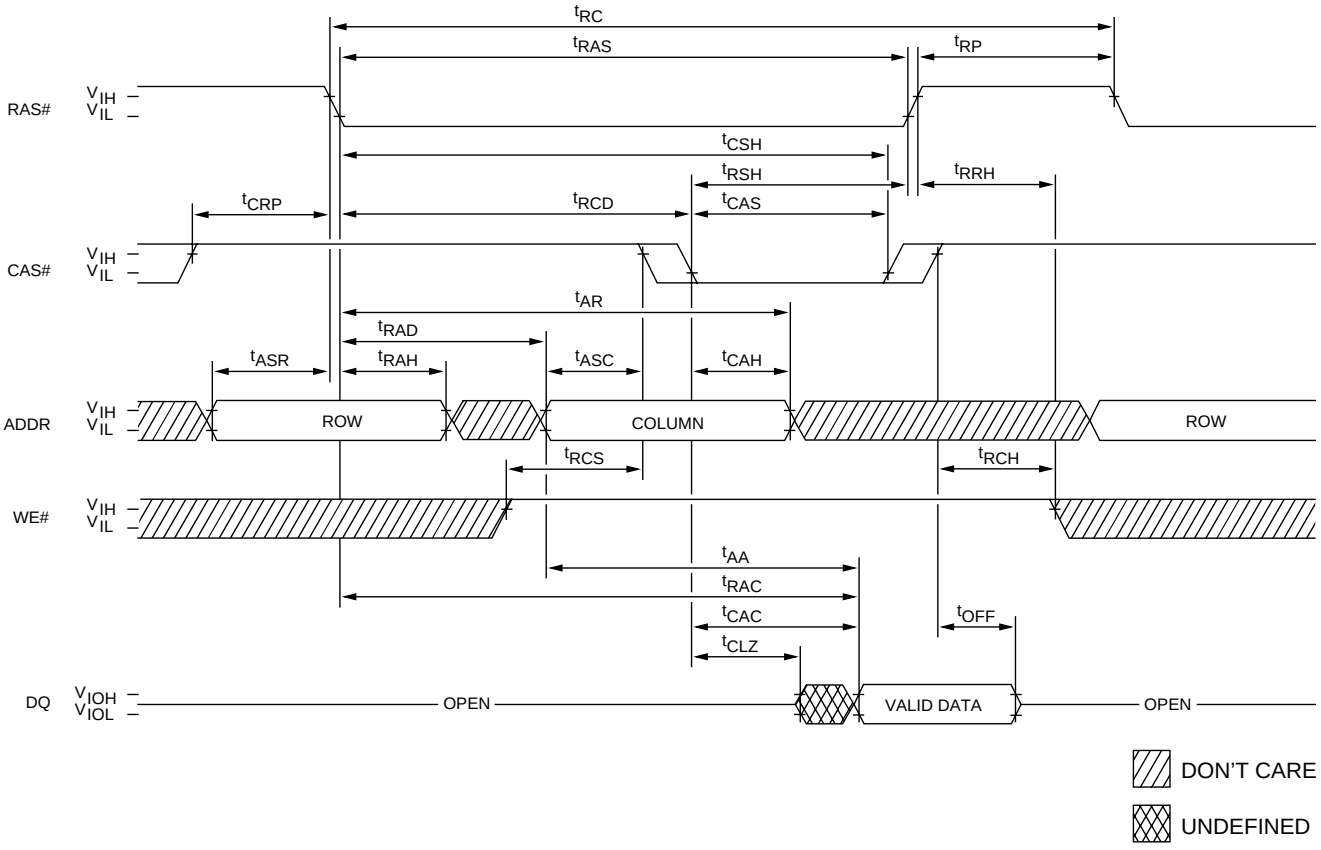
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command hold time (referenced to RAS#)	^{t}RRH	0		ns	16
RAS# hold time	^{t}RSH	15		ns	
Write command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	2	50	ns	
Write command hold time	^{t}WCH	10		ns	
Write command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	
Write command pulse width	^{t}WP	10		ns	
WE# hold time (CBR REFRESH)	^{t}WRH	10		ns	
WE# setup time (CBR REFRESH)	^{t}WRP	10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{CC} = 4.5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 16MB module values will be half of those shown.

READ CYCLE

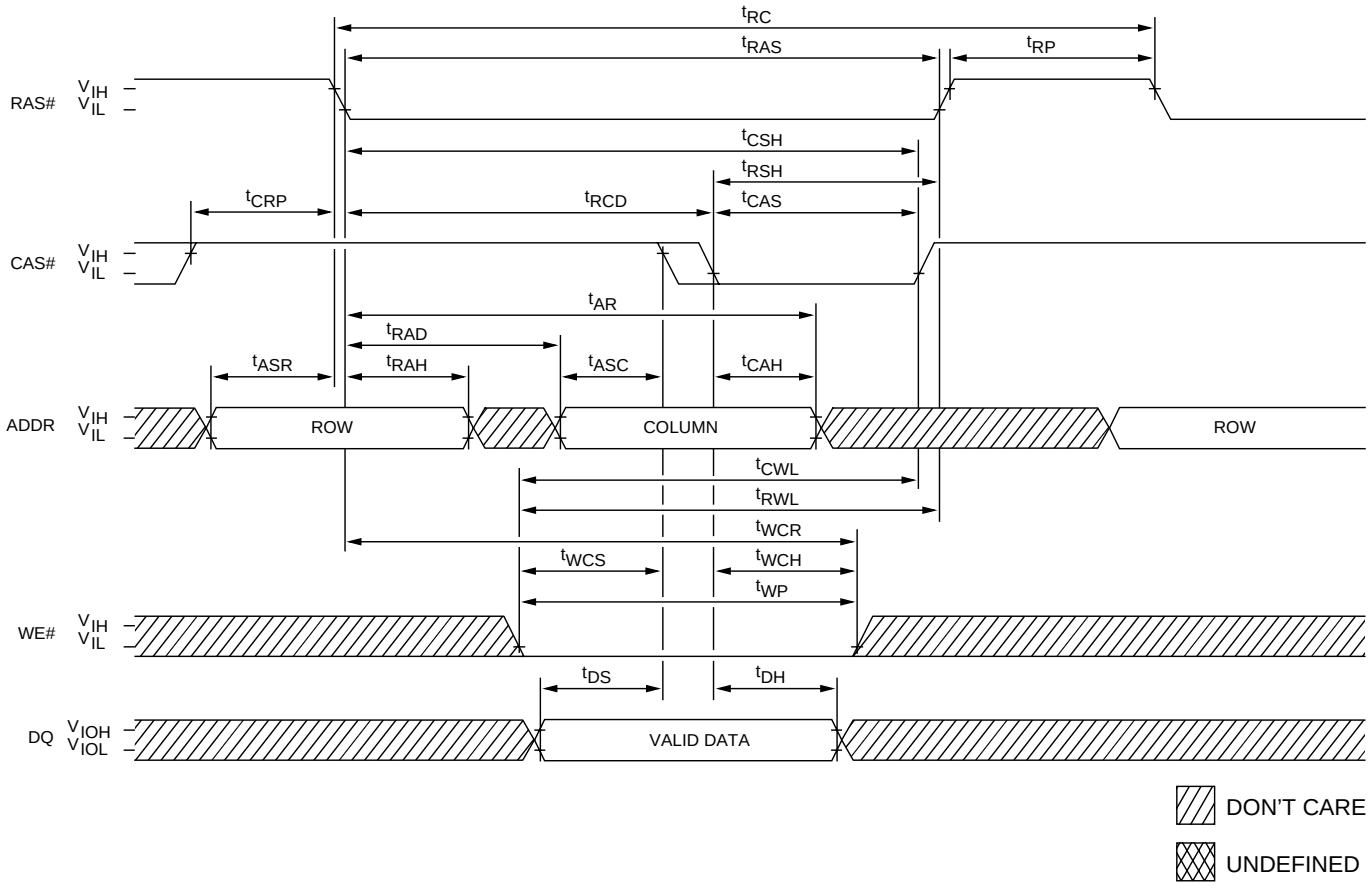


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCRP	10		ns
tCSH	60		ns
tOFF	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EARLY WRITE CYCLE

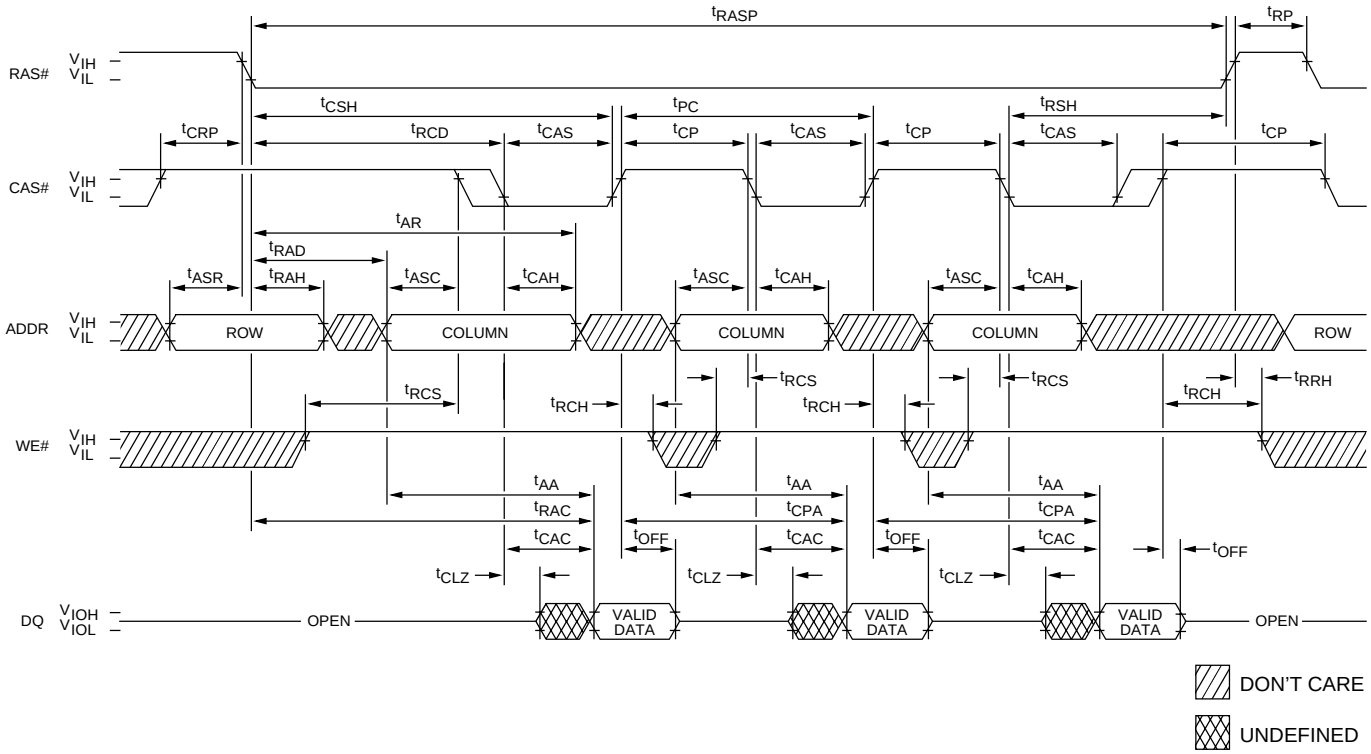


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tRAD	15		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

FAST-PAGE-MODE READ CYCLE

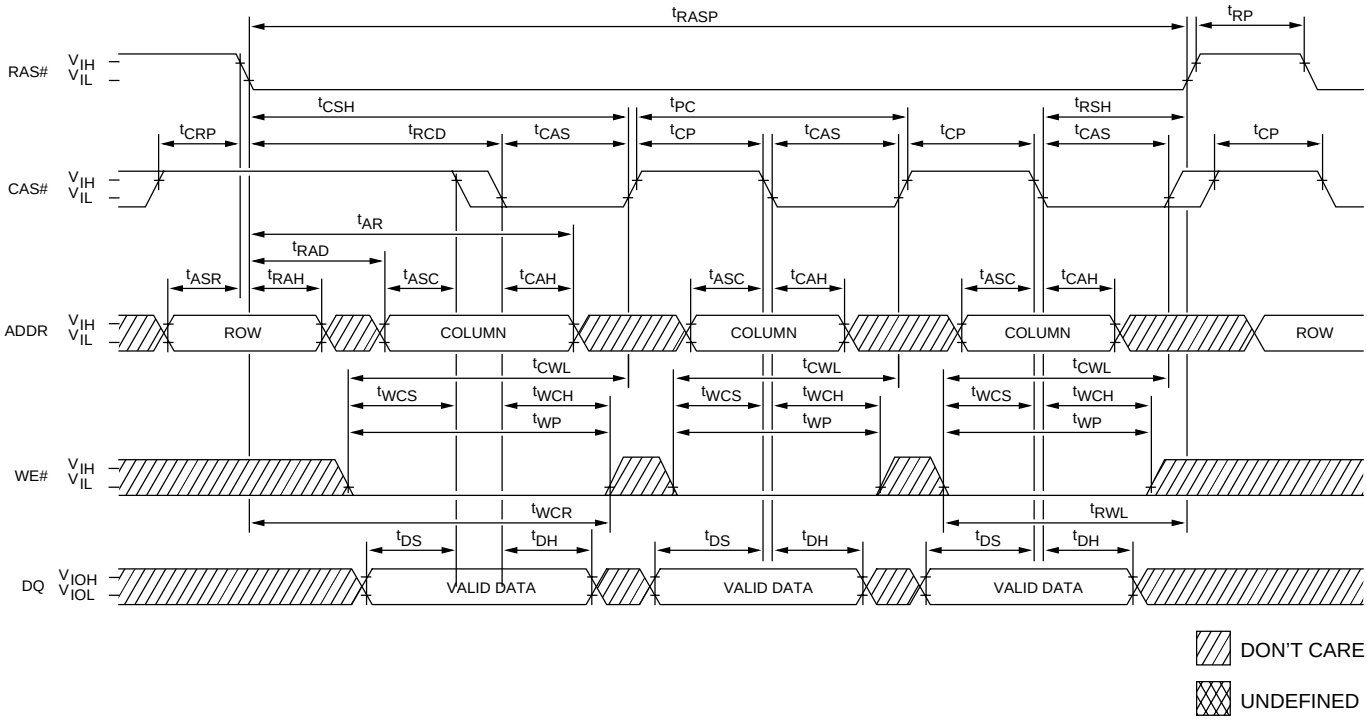


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

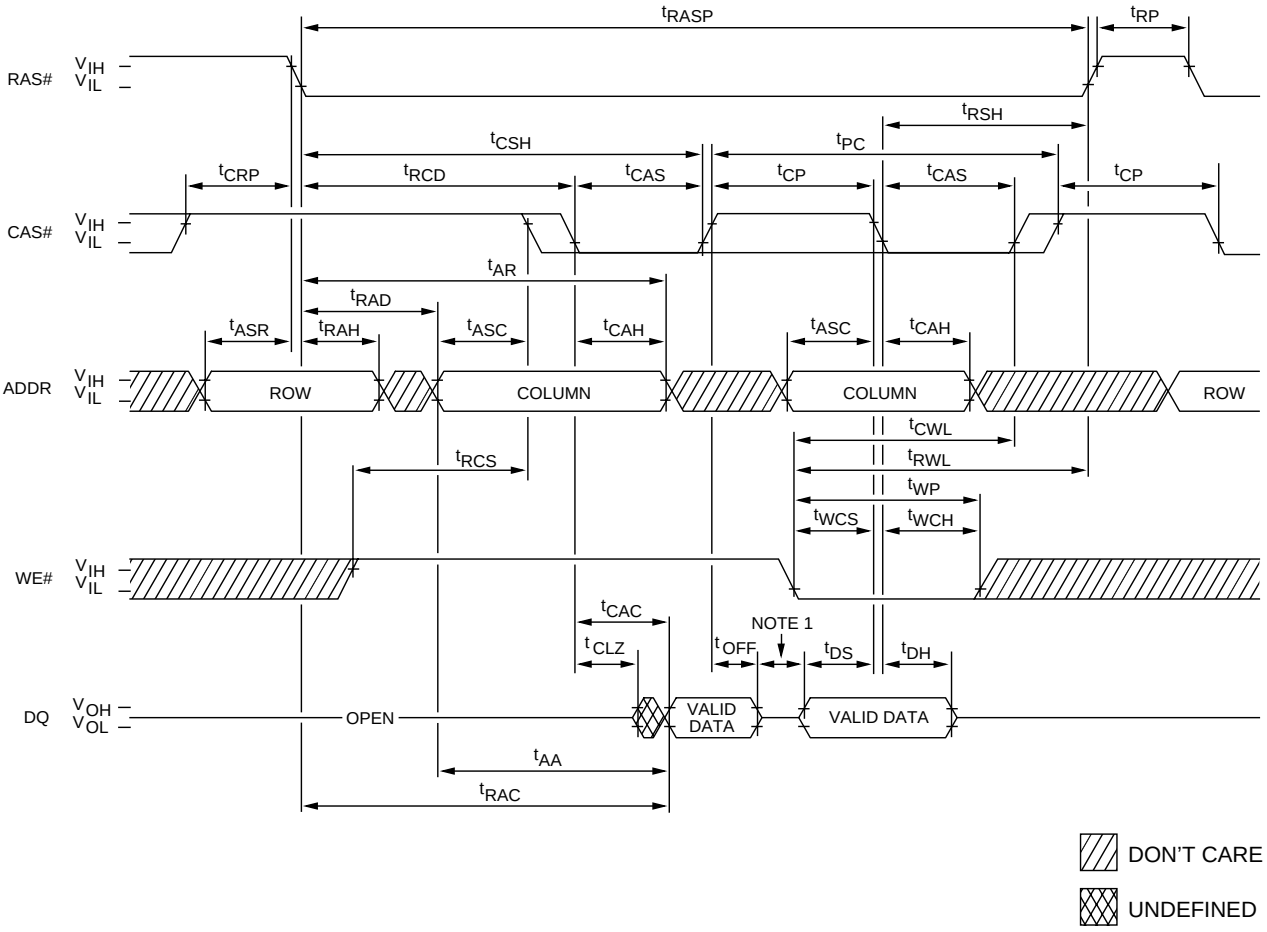


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCP	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tPC	35		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



TIMING PARAMETERS

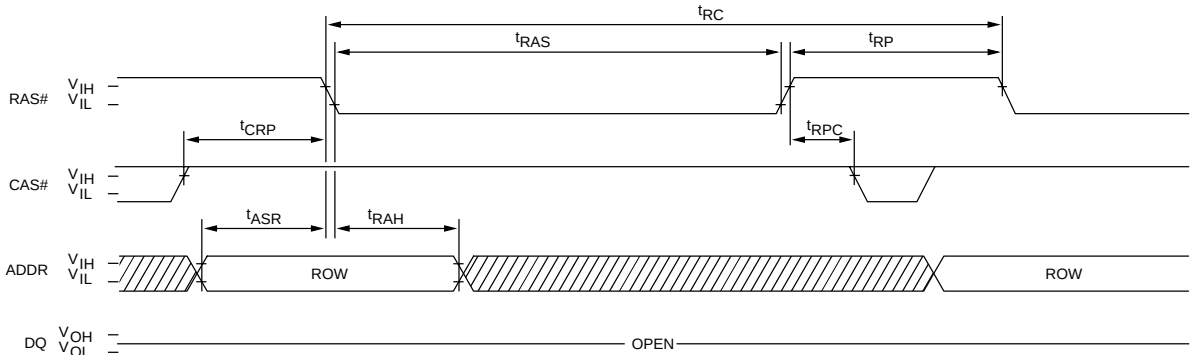
SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

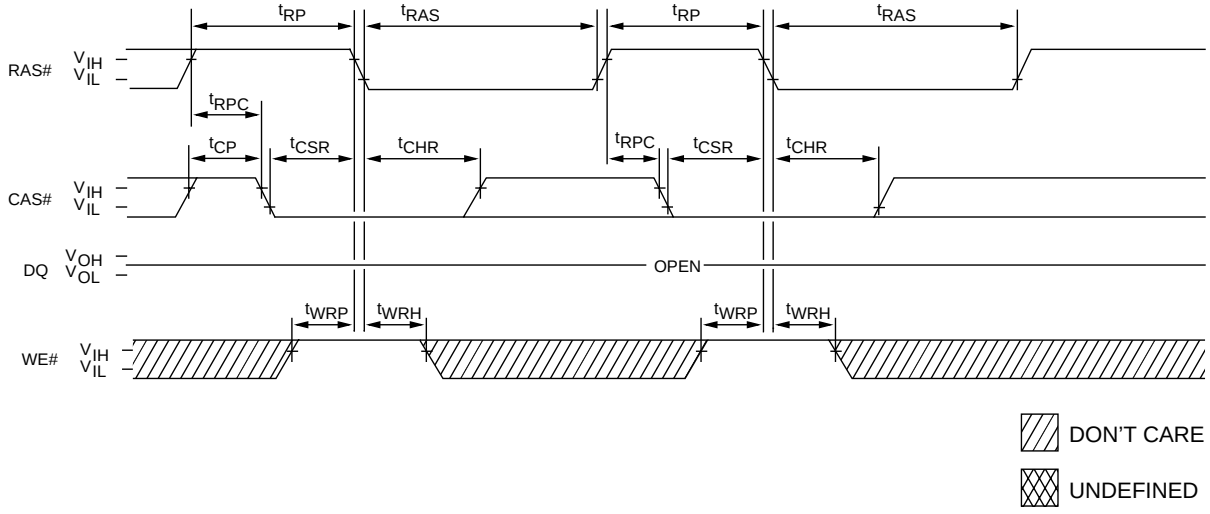
RAS#-ONLY REFRESH CYCLE

(WE# = DON'T CARE)



CBR REFRESH CYCLE

(Addresses = DON'T CARE)

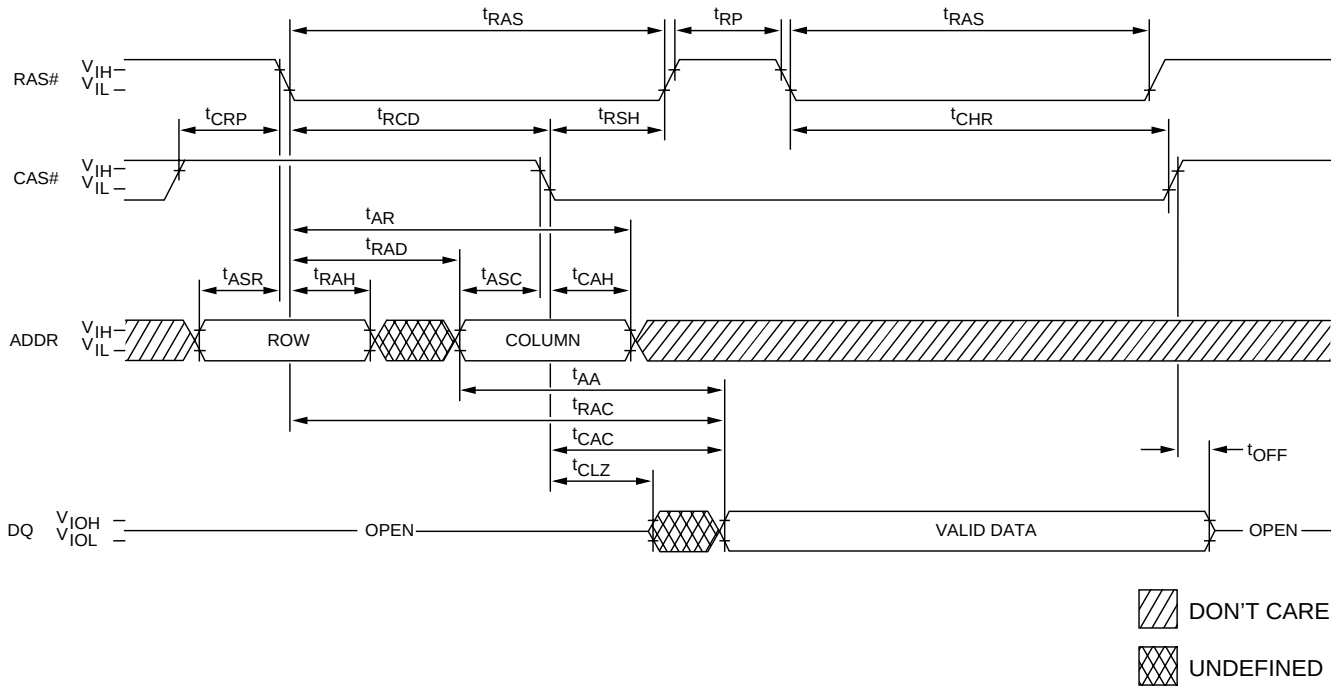


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tASR	0		ns
tCHR	15		ns
tCP	10		ns
tCRP	10		ns
tCSR	10		ns
tRAH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAS	60	10,000	ns
tRC	110		ns
tRP	40		ns
tRPC	0		ns
tWRH	10		ns
tWRP	10		ns

HIDDEN REFRESH CYCLE [20]
(WE# = HIGH)

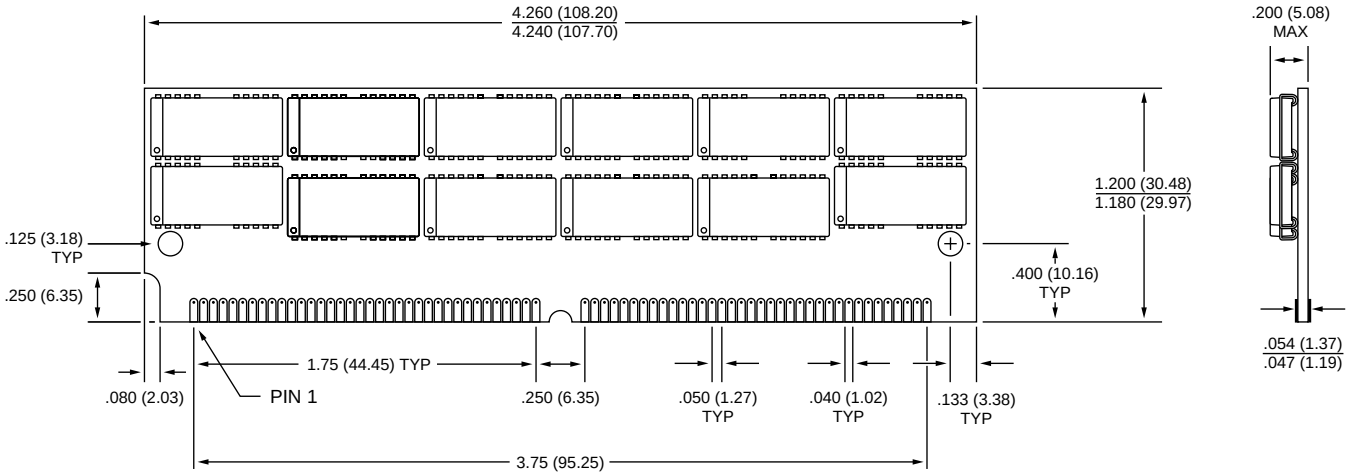


TIMING PARAMETERS

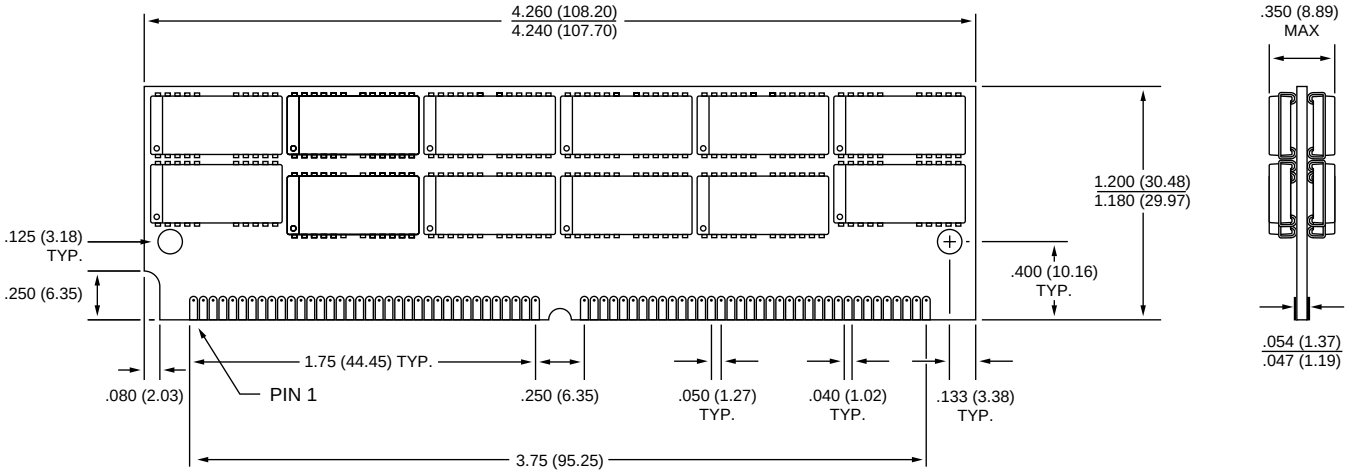
SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCHR	15		ns
tCLZ	3		ns
tCRP	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns

72-Pin SIMM
(16MB)



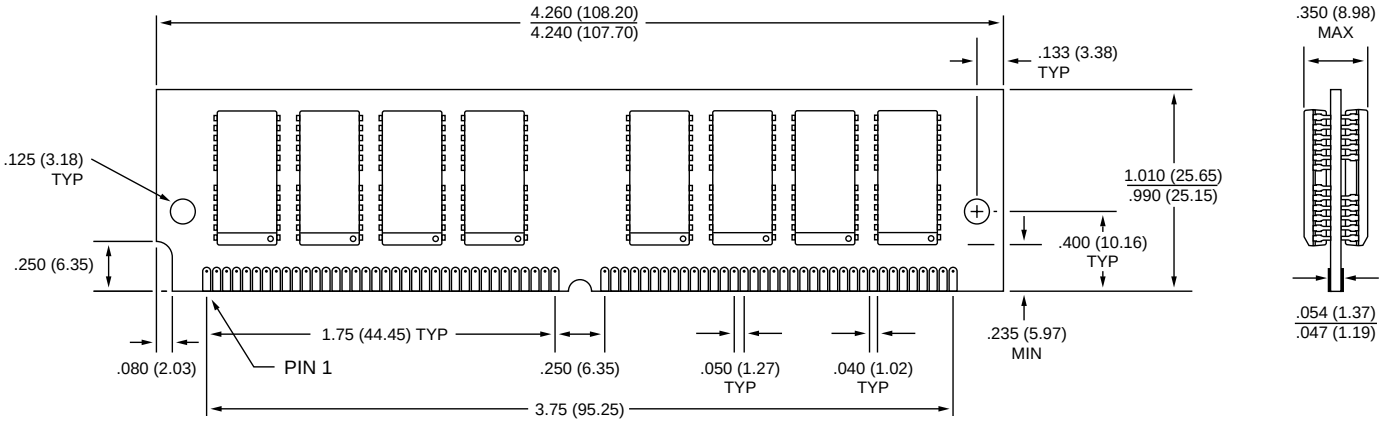
72-Pin SIMM
(16MB)



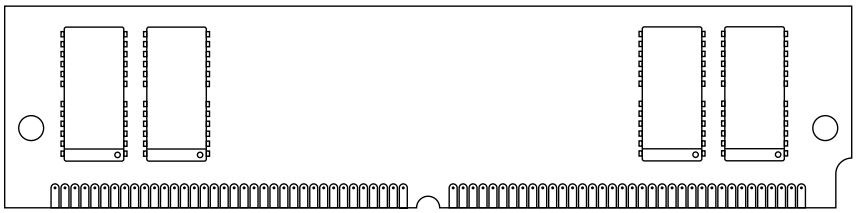
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

72-Pin SIMM
(32MB)

FRONT VIEW



BACK VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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