CMSC313 - Summary of Learning Objectives

Declare the 3 different forms of digital logic
Draw simple electronic logic gate circuits for AND, OR, NOT, NAND, NOR
Identify logic gate symbols and their corresponding functions
Interpret Boolean expressions written in software form
Synthesize composite combinational functions
Develop truth tables from gate level diagrams
Compile a truth table for all possible functions of two binary variables
Define and apply the following terms for logic design : Logic Threshold, Buffer, Bubble Matching, Positive and Negative logic, Minterms and Maxterms
Simplify Boolean Algebra expressions using laws of Boolean Algebra
Develop combinational logic solutions in SOP and POS form
Configure positive and negative logic circuits

Describe and apply the listed functions: Multiplexer, Demultiplexer, Decoder, Priority Encoder, Programmable Logic Array
Design a ripple carry adder using digital components described
Name the 3 methods of logic reduction
Reduce logic expressions and circuits using Boolean algebra theorems, Karnaugh-Maps, OR gate and MUX decomposition
Draw a ripple carry adder block diagram
Devise a ripple carry subtractor
Draw a circuit that combines the processes of ripple carry addition and subtraction
Develop equations for a carry look ahead adder given basic G (generate)and P (propagate) identities
Determine maximum and minimum gate delays in the carry look ahead adder

Draw up truth tables for D/ S-R / T and J-K FF's
Generate excitation tables for the listed FF's
Draw a block diagram of a general FSM
Design a finite state machine from a functional description
State the differences between Mealy and Moore FSM's
Understand how register structures work
Build up module 2N counters using JK FF's
Use state reduction to simplify FSM's

Identify critical parameters for logic gates and components from their datasheets
Interpret characterizations of propagation delays for a gate
Understand how different kinds of computer memory are arranged
Describe 3 different memory communications techniques
Know the different arrangements used in cache architectures
Calculate hit ratios for memory caches