CMSC313 Fall 2003
In Class Lab #2
Introducing the JK Flip-Flop

Objectives

Review the operation of a JK flip-flop circuit. Implement a clocked JK flip-flop using 74 series gates. Verify the truth table using this circuit.

Procedure

[1] Write your name on each paper in this handout in the top left hand corner. Complete the JK flip flop (FF) truth table in the space provided in figure 1. Qn+1 is the state of the Q output after clocking the FF.

[2] Examine the schematic shown in figure 2. Identify any inconsistencies in the schematic. Identify the functions of logic gates sets {U1a, U1c, U2a, U2c} and {U2b, U2d} in the schematic shown in figure 2. Is there a better type of JK FF circuit? State your reasons.

[3] Assign the available {J,K} input combinations to each logic circuit in Appendix A and verify that the Q and QB outputs are in agreement with the JK FF truth table.

[4] Check that you have the following items for building the circuit:

Universal electronic breadboard	Battery pack with switch
DIL quad switch module	LED
Diode 1N4148 or equivalent	One (1) off 74LS00 Quad NAND gate IC
Two (3) off 4.7 kΩ resistors	One (1) off 74LS08 Quad AND gate IC
Two (2) off 270Ω resistor	Prototyping wire

[5] Having identified the inconsistencies in the schematic, correct it and assign pin numbers for gate to gate connection. Connect up (DO NOT POWER UP) the circuit shown in figure 2. Use the copy of your corrected schematic shown in Appendix B to record each step of your breadboard circuit build.

[6] Establish the initial state of the inputs J, K and CLK in your circuit using the switches.

[7] Carefully check the rest of the circuit's connections. Power up the circuit.

[9] Feed the circuit it with different values of the logic inputs as follows: Make sure that the switch for CLK is set to logic '0'. Set the switches which assign the J and K inputs. Once you have done this, clock the flip flop by raising and then lowering the logic level of the clock using the appropriate switch; Record a test output truth table that is being produced, corresponding with the values of Q and QB you observe. Repeat the process until all the legal JK input combinations have been tried.

[10] Write down your observations and make conclusions about the experiment in Appendix C on page 5.

Qn	J	K	Qn+1
0			
0			
0			
0			
1			
1			
1			
1			

Figure 1 JK FF Truth Table

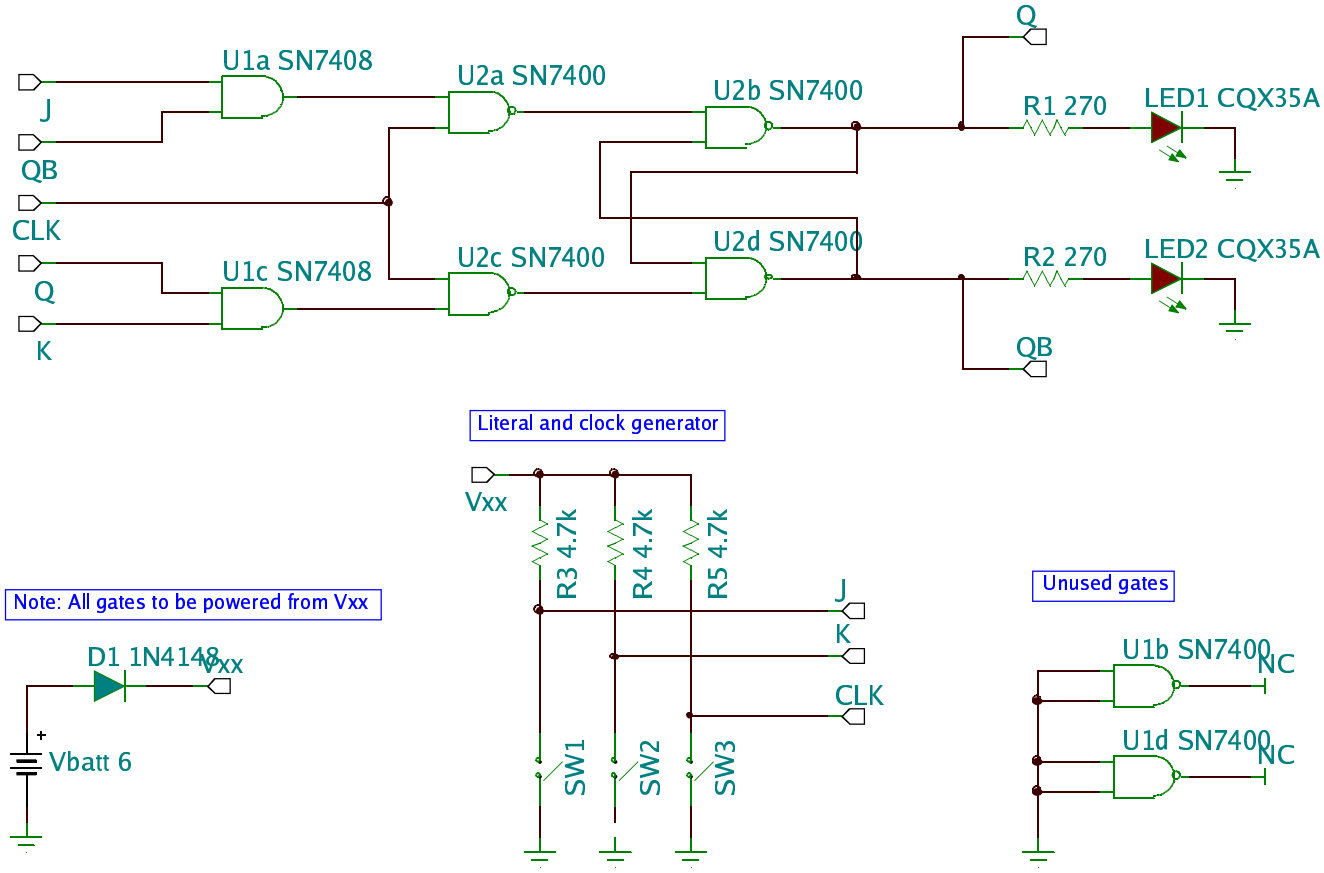
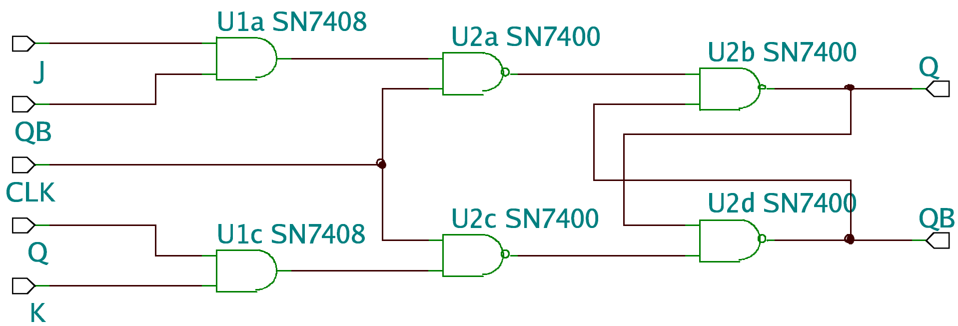
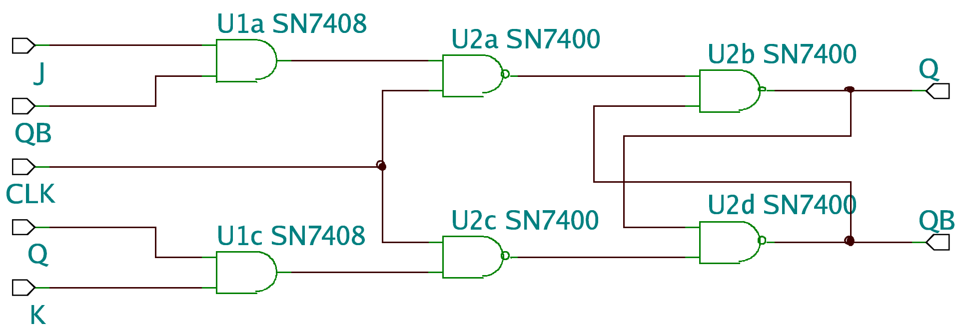
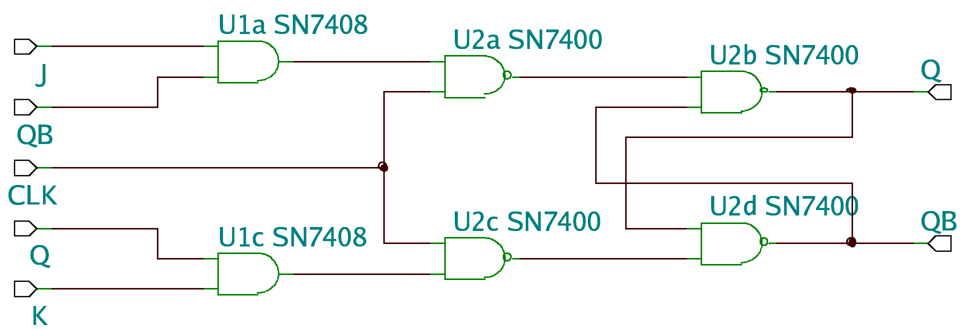


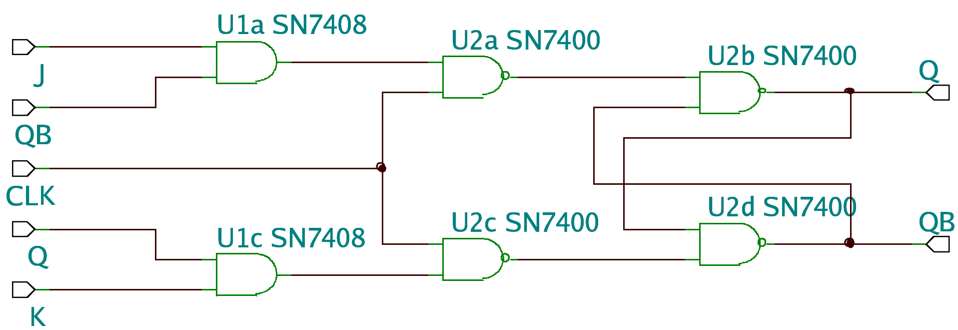
Figure 2 Experimental Logic Schematic

Appendix A JK FF Functional Verification

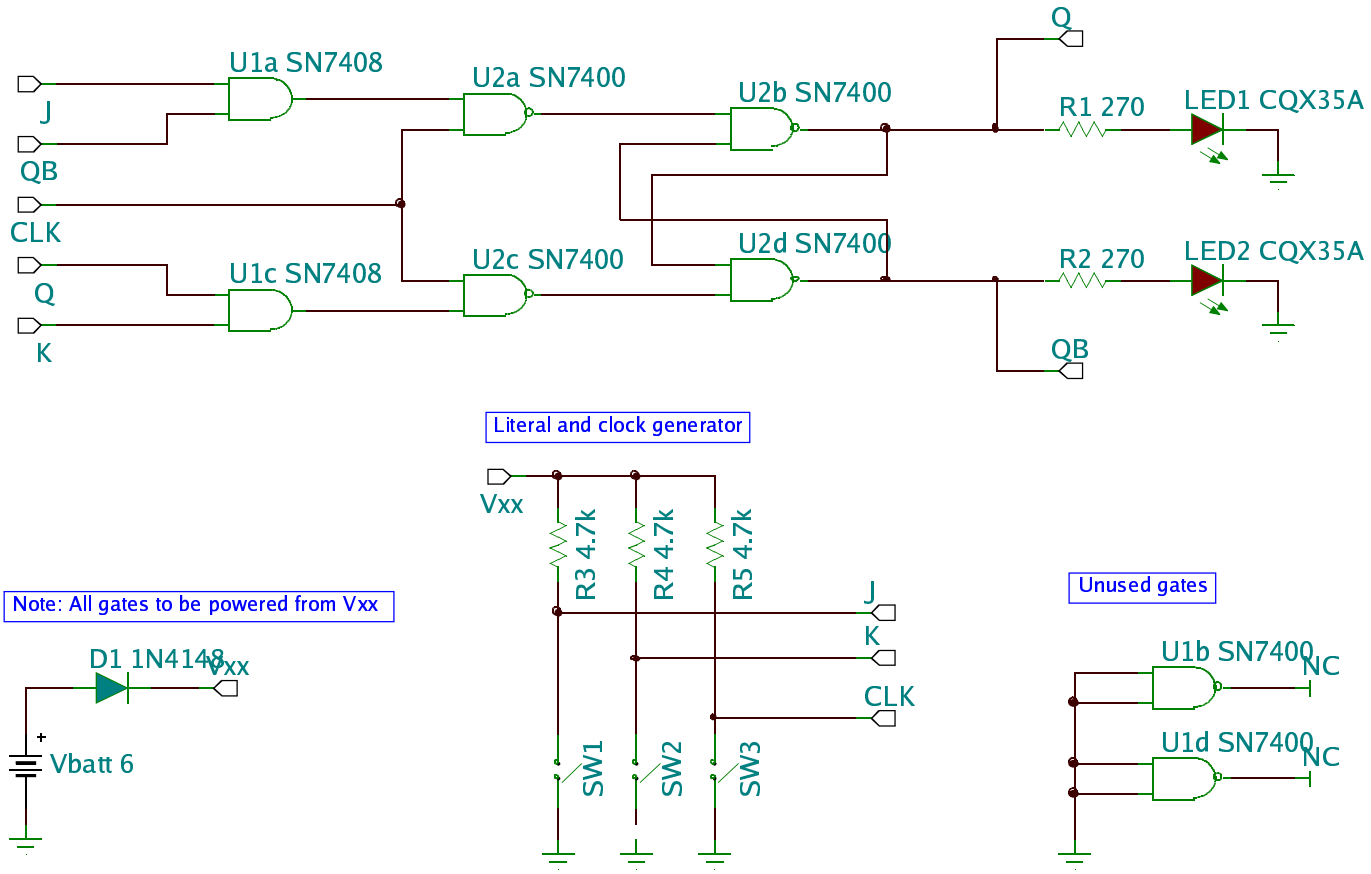








Appendix B Circuit Build Checking Schematic



Appendix C – Experimental Notes

Observations

Conclusions