

Homework #3

PROBLEMS in approved textbook (note 1) following Appendix A

- {1} A.3 [10]
- {2} A.10 (We viewed a circuit like this, used for comparing letters, in the video in last week's lecture) [20]
- {3} Draw schematics for the following functions using AND, OR and NOT gates. Do not simplify the formulas.
- $X(Y + Z)$
- $X+YZ$
- $X(Y + Z)$
- $W(X + YZ)$
- Draw circuit solutions for (a) and (d) that each incorporate a single tristate buffer. [30]
- {4} For each CMOS circuit (figures 1 and 2 in the appendix below),
- (a) Provide a truth table for the circuits' functions
 - (b) Draw the logic diagram of the functions using AND OR NAND NOR and NOT gates.
- [20]
- {5} It is required to design a lighting circuit for a warehouse such that the lights may be switched on or off from any one of three switch points. Set up the truth table for the problem and derive the corresponding switching equation. Simplify this equation if possible and draw the resulting logic gate circuit. [10]
- {6} View the circuit, shown in figure 3 of the appendix. Note that the dots indicate connections between the lines as they cross each other. Assume that the inverters, 2-input AND, 3-input AND and OR gates have propagation delays of 10ns, 18ns, 22ns and 14 ns respectively. Assume that the delays associated with interconnect can be neglected. What is the minimum and the maximum expected propagation delay in this circuit? [10]
- Total [100]**

Notes: (1) Approved textbook: "Principles of Computer Architecture" M J Murococa & V P Heuring Prentice Hall 2000 ISBN 0-201-43664-7

Computer Organization and Assembly Language Programming (CMSC 313)
Section 0102 Fall 2003

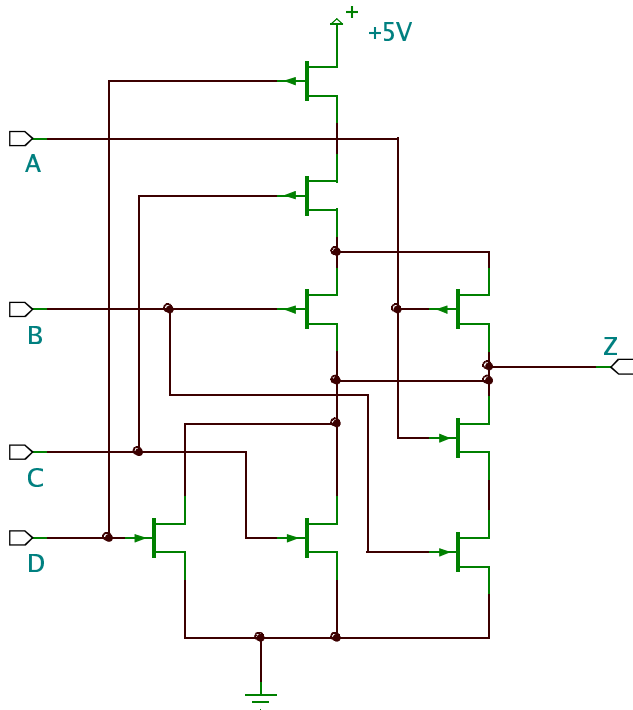


Figure 1

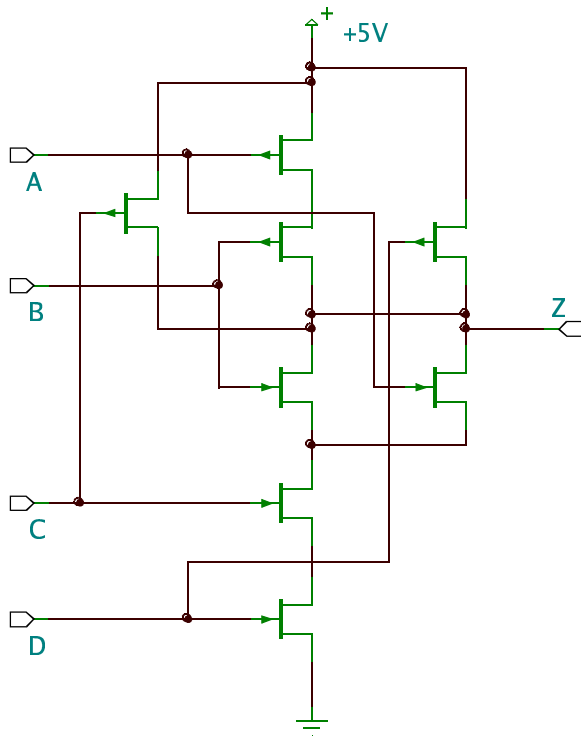


Figure 2

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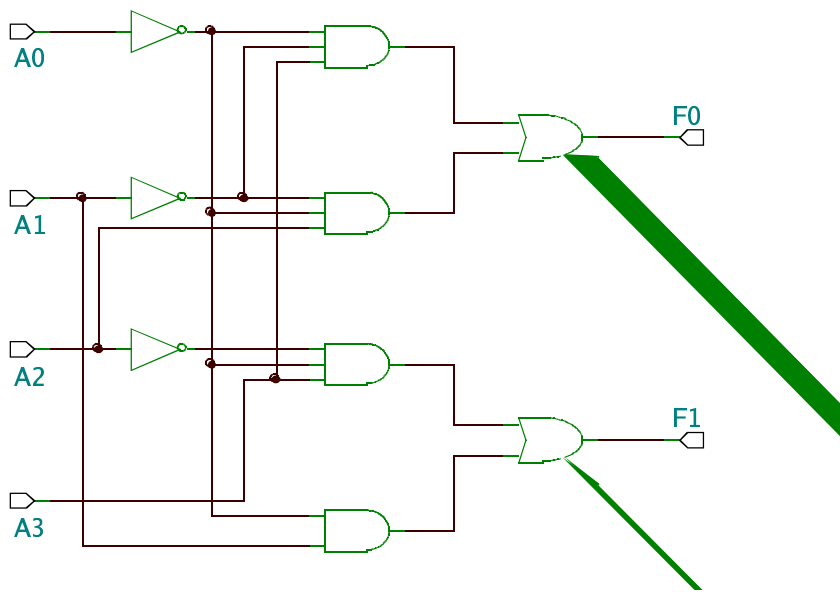


Figure 3