Test Economics

Engineers concerned with optimizing technological efficiency.

Economists prefer to minimize cost.

Fixed and variable costs of material, equipment, labor, etc. are important.

Test economics focuses on the relationship between ***testing cost*** and ***product quality***.

The relationship is complex.

For complex systems, testing cost is > 30% of the total cost.

Testing is responsible for the quality of VLSI chips.

Goal: obtain *required* quality level at *minimum* cost.

Costs include:

- Cost of ATE (initial and running).
- Cost of test development (CAD tools, test generation, test programming).
- Cost of DFT (scan reduces cost of test generation, BIST reduces complexity and cost of ATE, both reduce yield however).

Yield

Process yield: Fraction of acceptable parts among all parts fabricated.

Wafer yield: average number of good chips/wafer.

Normalizing wafer yield by the # of chip sites on the wafer can be used as process yield.

Many factors affect ***yield*** including *die area*, *process maturity* and *number of process steps*.

It is difficult to obtain an exact value of yield:

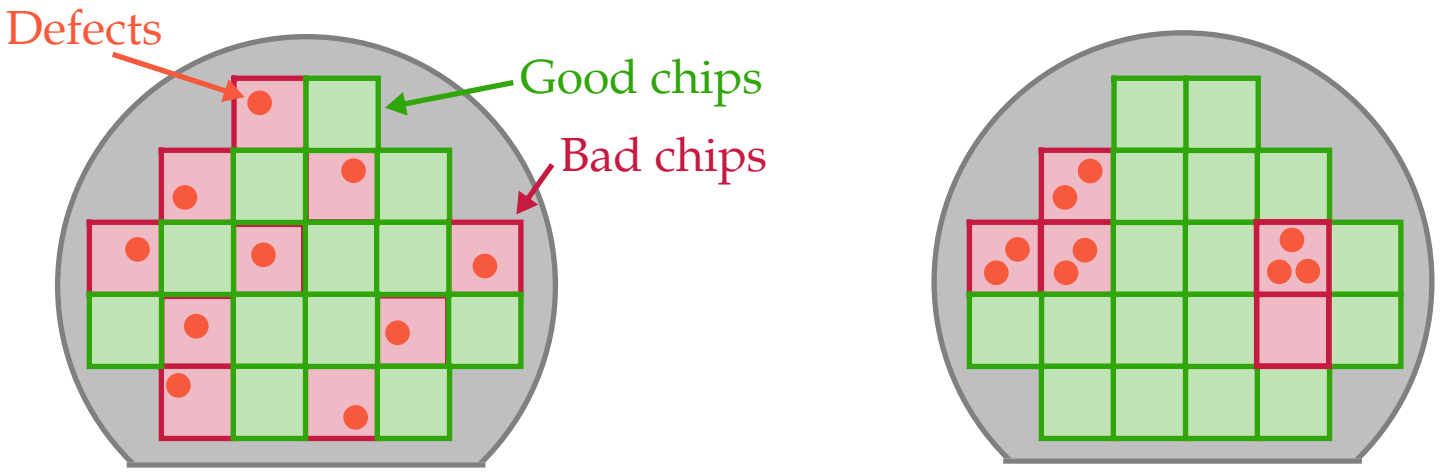
- Tests are based on fault models that do not detect all defects.
- Lack of data once the product is sold.

Defect Level (DL) are the fraction of bad chips that pass final package tests.

DL is usually expressed in ***Defect-Per-Million*** or ***DPM***.

Defect Modeling

Two scenarios for defect modeling:



Unclustered defects

Wafer yield = 12/22 = 0.55

Clustered defects

Wafer yield = 17/22 = 0.77

Fortunately, clustered defect model better represents reality.

Random defects are characterized by two parameters:

- defect density, d, which is the average number of defects per unit area.
- clustering parameter, a.

The average number of defects on a chip of area A is Ad.

Defect Modeling

In any random chip, the number of defects, x, is an integer-valued random variable.

Defect clustering is best modeled assuming a ***negative binomial*** probability density function for x:

$$p(x) = Prob(\#\text{ of defects on chip=x})$$

$$p(x) = \frac{\Gamma(\alpha + x)}{x!\Gamma(\alpha)} \frac{(Ad/\alpha)^x}{(1 + Ad/\alpha)^{\alpha + x}} \qquad (1)$$

where $\Gamma(x)$ is the *gamma function* given by

$$\Gamma(x) = \int_0^\infty e^{-x} x^{n-1} dx$$

The mean, $E(x)$, and variance, $\sigma^2(x)$ are defined as:

$$E(x) = Ad$$

$$\sigma^2(x) = Ad(1 + Ad/\alpha) \qquad (1a)$$

Yield Models

In order to predict the yield, we need the ***mean*** and ***variance*** for the number of defects on a chip.

Obtain either from experimental measurements or process simulation.

Substitution of the mean and variance in equations *(1a)* gives yield parameters, d and a.

Yield is obtained as the probability, $p(0)$, of no defect on a chip.

Substituting x=0 into the equation *(1)* gives:

$$Y = (1 + Ad/\alpha)^{-\alpha} \qquad (2)$$

For the ***unclustered*** model:

$$\alpha \to \infty \Rightarrow p(x) = \frac{(Ad)^x e^{-Ad}}{x!}$$

with x = 0, the yield is: $Y_{\text{Poisson}} = e^{-Ad}$ (3)

Yield Models

However, this model predicts low yields.

If $Ad = 1.0$ and a = 0.5 (typical of a large VLSI chip) then using *(3)*:

$$Y_{\text{Poisson}} = \frac{1}{e} = 0.37 \qquad (4)$$

Using *(2)*, a more realistic prediction of 0.58 is obtained.

Yield may be low when fabricating a new design, and more accurately predicated by *(3)* than by *(2)*.

Consider the impact of testability (the cost of testability overhead):

- $d = 1.25$ defects/cm^2
- a = 0.5
- chip area, A, is 8mm X 8mm = 0.64cm^2.

Equation *(2)* gives:

$$Y = \left(1 + \frac{0.64 \times 1.25}{0.5}\right)^{-0.5} = 0.62$$

Example

Now suppose:

- The process uses 8-inch wafers
- The cost of processing a wafer is $100
- Each wafer has 400 chips

Processing cost per chip is:

$$\text{Cost}_{chip} = \frac{\$100}{(400 \times 0.62)} = 40 \text{ cents}$$

Assume the chip size increases by 10% after DFT is included. Yield is then:

$$Y_{DFT} = \left(1 + \frac{0.64 \times 1.10 \times 1.25}{0.5}\right)^{-0.5} = 0.60$$

2% reduction in yield

With DFT, a wafer contains 400/1.1 ~= 364 chips. Therefore, processing cost is:

$$\text{Cost}_{chip} = \frac{\$100}{(364 \times 0.60)} = 46 \text{ cents}$$

15% increase over no DFT

DL and Quality

DL (or reject ratio) is a measure of the effectiveness of the tests.

Objective is to develop a test that reduces the number of outgoing faulty parts to an acceptable level

It's too expensive to try to get them all.

The DL can be determined from the field return data.

Chips are returned if they fail acceptance test, fail system test or fail in the field during a maintenance test.

For commercial VLSI chips, a DL *>500ppm* is considered unacceptable.

Actual DL is difficult to determine:

- Some failed parts are not returned
- Some returned parts are damaged in handling
- It takes a long time (a year) to collect sufficient data
- The DL reduces over time

Therefore, computed DL is usually overly pessimistic.

Test data analysis from manufacturing test data gives estimate.

Estimating Defect Level

The yield equation *(1)* can be modified to do this.

- Fault density (as opposed to defect density) defined as f = average number of SA faults per unit chip area.
- Fault clustering parameter, b
- Stuck-At fault coverage, *T*.

$$Y(T) = (1 + TAf/\beta)^{-\beta}$$

Here, we obtain the 'measured' yield when a test with fault coverage T is applied.

Assume that tests with 100% fault coverage (T=1.0) remove all faulty chips:

$$Y = Y(1) = (1 + Af/\beta)^{-\beta} \qquad (5)$$

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)} = 1 - \left(\frac{\beta + TAf}{\beta + Af}\right)^{\beta} \qquad (6)$$

(multiply by 10^6 to get PPM).

Af (average number of faults) and b are determined from test data.

Estimating Defect Level from SEMATECH data

This model can be evaluated on IBM′s SEMATECH data.

CUT characteristics:

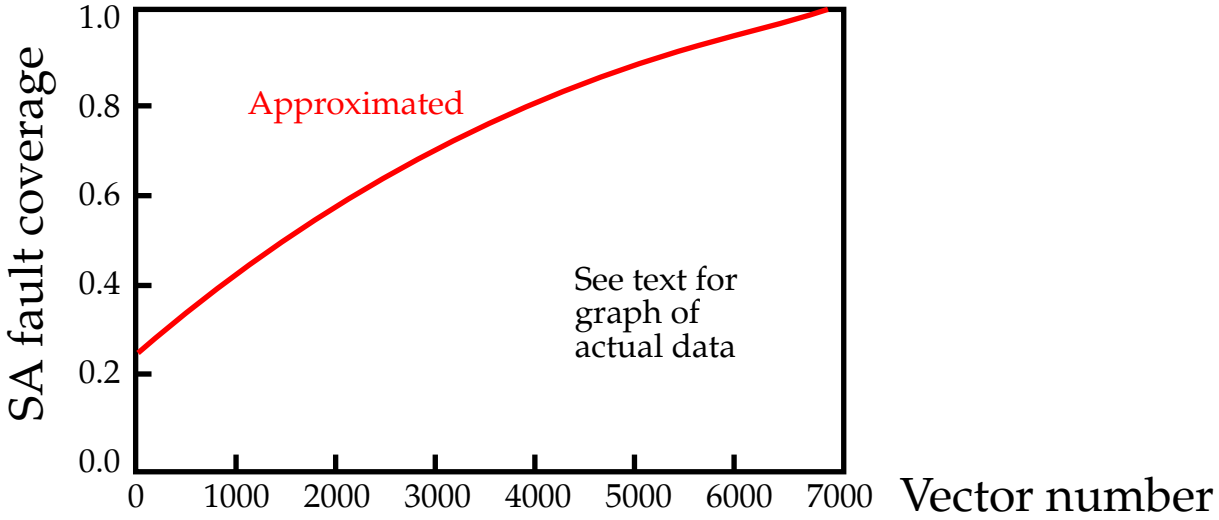
- CUT is a bus interface controller ASIC containing 116,000 equivalent 2-input NAND gates.
- CUT has 249 I/O and a 304-pin package.
- Some portions of chip operate at 40MHz, others at 50MHz.
- Full scan, with 5,280 scan latches.
- 3.3V power supply, 3 metal, 0.45um technology, 9.4mm x 8.8 mm die size.
- Four types of tests applied, SA, functional, delay and I_{DDQ}.

  IBM′s LSSD scan chain design allows a scan flush test.
- With scan tests, total SA coverage was 99.79% for a total of 375,142 faults.
- Advantest 3381 ATE used.
- 18,466 chips tested at 2.5MHz test clock.

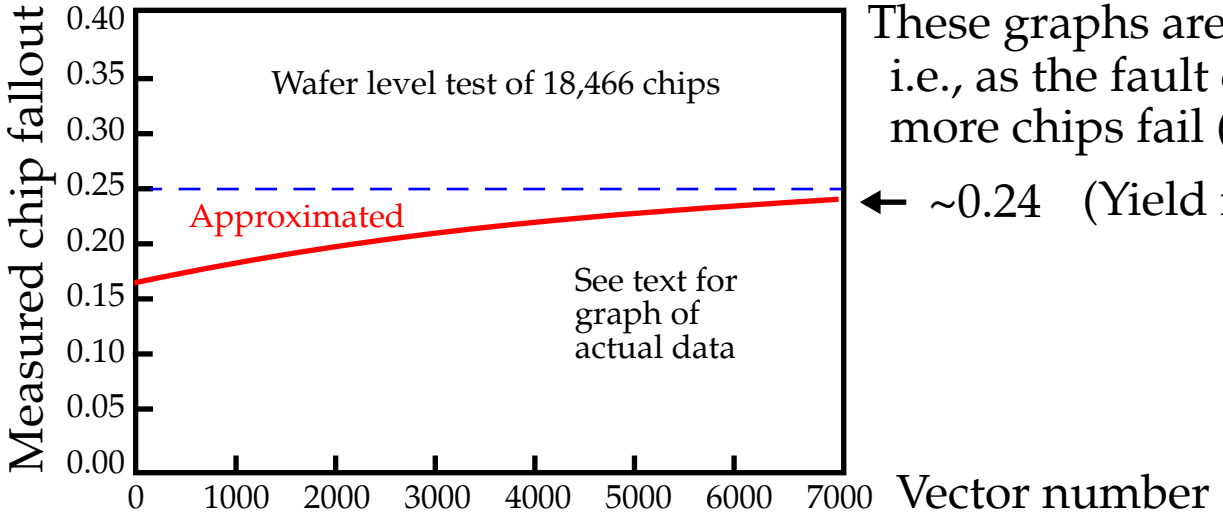
  (Data provided courtesy Phil Nigh, IBM).

Estimating Defect Level from SEMATECH data

Fault coverage computed using a fault simulator:



Chip fallout vs. test vector number:

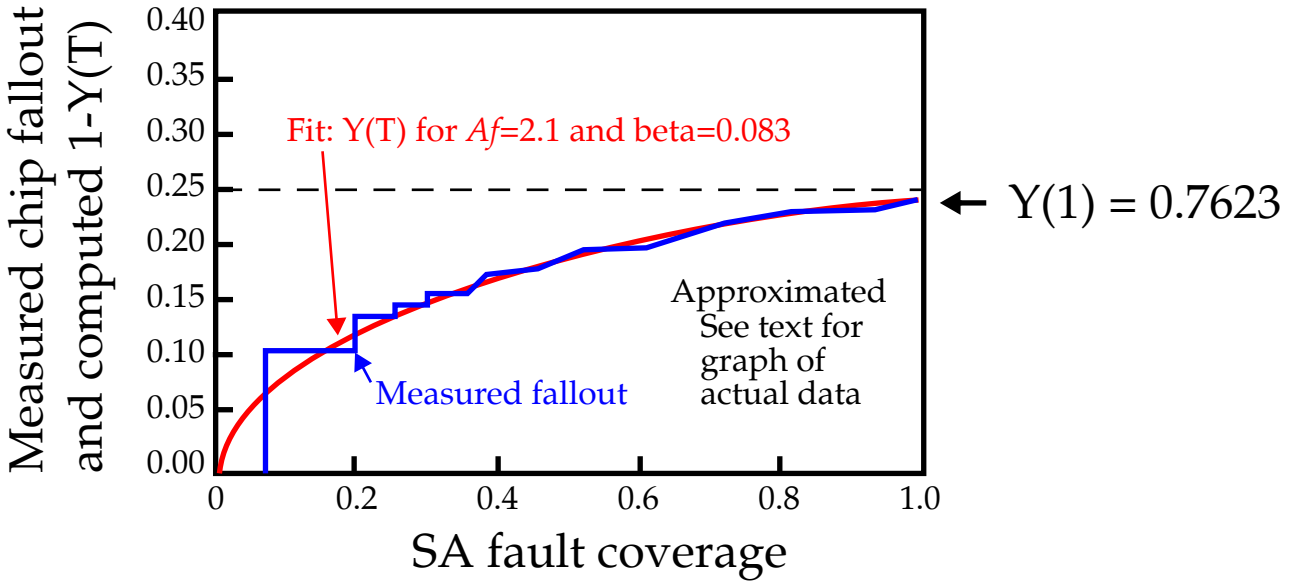


These graphs are consistent, i.e., as the fault coverage rises, more chips fail (**fallout**).

← ~0.24 (Yield is ~76%)

Estimating Defect Level from SEMATECH data

The data from the two graphs can be plotted and fitted.



Plotted fallout rate function, 1 - Y(T), given by:

$$1 - Y(T) = 1 - [1 + TAf/\beta]^{-\beta}$$

Fitting yields A*f*=2.1 and b=0.083.

This gives $f = Af/A = 2.1/(0.94*0.88) = 2.54$ faults/sq. cm.

Using these values, Eq *(5)* gives Y = 76.23 and *(6)* gives DL = 168 for T=0.9979

Estimating Defect Level from SEMATECH data

This type of analysis allows the yield and fault distribution parameters to be determined.

The fab process must be diagnosed and corrected if they are not as expected.

Also, if the defect level is too high, the fault coverage of the patterns must be improved.

Bear in mind, the tests in this study were run at slow speed.

Therefore, some chips that passed have delay faults.

Other tests may be necessary to make other defects have a non-zero probability of detection.

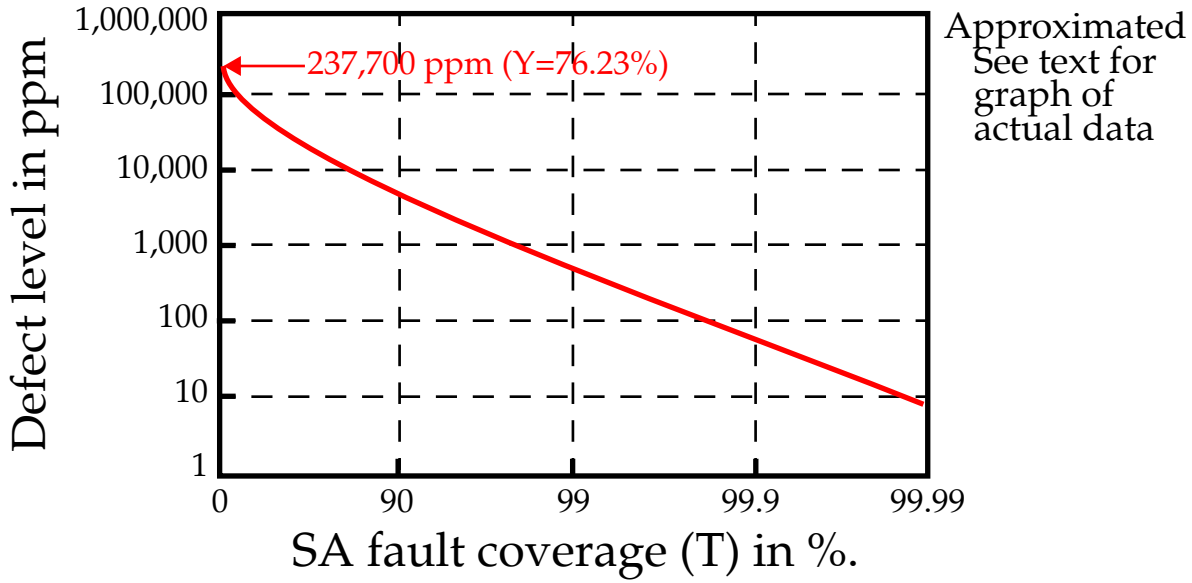
Deriving better tests is the focus of some recent research.

Eq *(6)* can be used to plot DL as a function of fault coverage.

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)} = 1 - \left(\frac{\beta + TAf}{\beta + Af}\right)^{\beta}$$

Estimating Defect Level from SEMATECH data

Note, a reverse logarithmic scale is used for the x-axis.



For zero fault coverage, the DL is 237,700 ppm.

Therefore, the lot of chips contains 76.23% good chips.

For fault coverage at 99%, DL reduces to <1000 ppm.

For 99.9% -> <100 ppm, for 99.99 -> <10ppm.

Remember, these DLs are realistic only if testing emulates real conditions.

Another view: these are the DL if the chips **are used** at 2.5MHz.

Yield and Testing

Testing cannot improve process yield.

It is only a screening process for bad chips.

Process yield can be improved by:

- Diagnosis and Repair

  Parts that fail Go/No-Go can be diagnosed and repaired in some situations.

  This strategy improves yield but also increases production cost.

- Process Diagnosis and Correction

  Failure analysis determines the root cause and the process is *corrected*.

  Therefore, this strategy is more cost effective.