## *ATE for Manufacturing Test*

Major ATE Companies: Teradyne, Credence, Agilent, Advantest, NPTest ...

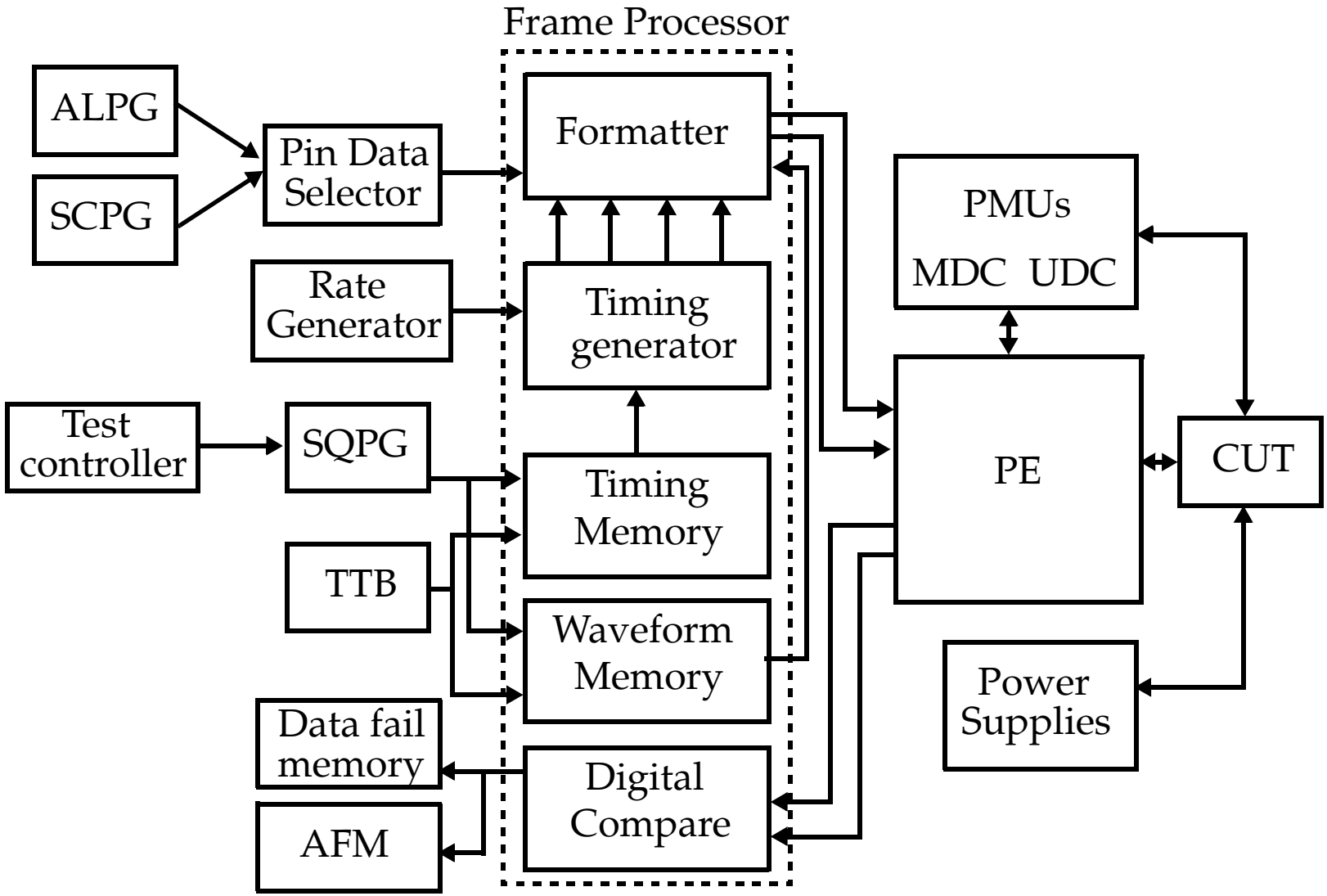
**Agilent 83K**



**Advantest T6682**

## *Block Diagram for T6682*

Block diagram for Advantest Model T6682 described in text:



## *T6682 Specifications and features*

- Chips in the tester itself are 0.35um technology.
- 1024 independently controllable and observable channels.
- Test speeds are 250MHz, 500MHz and 1GHz.
- Overall timing accuracy is +/- 200ps.
- Clock/strobe accuracy is +/- 870ps (80ps for AC measurements).
- Drive voltages are -2.5 to 6V.
- Pattern multiplexing (2 patterns written per ATE cycle) used for 500MHz.
- Pin multiplexing (2 tester channels drive one chip pin) used for 1GHz.

### *SQPG: Sequential pattern generator*

Stores 16 Mvectors of patterns (vector is # of CUT pins).

### *ALPG: Algorithmic pattern generator*

32 address bits, 36 data bits.

### *SCPG: Scan pattern generator*

Supports JTAG, boundary scan

## *T6682 Specifications and features*

### *Response checking*

- Pulse train matching: ATE matches bits on 1 channel over 16 cycles or less.

- Pattern matching mode: ATE matches multiple bits from CUT outputs.
  Compares with expected output.
  Result of compare can change the sequence of patterns in real time.

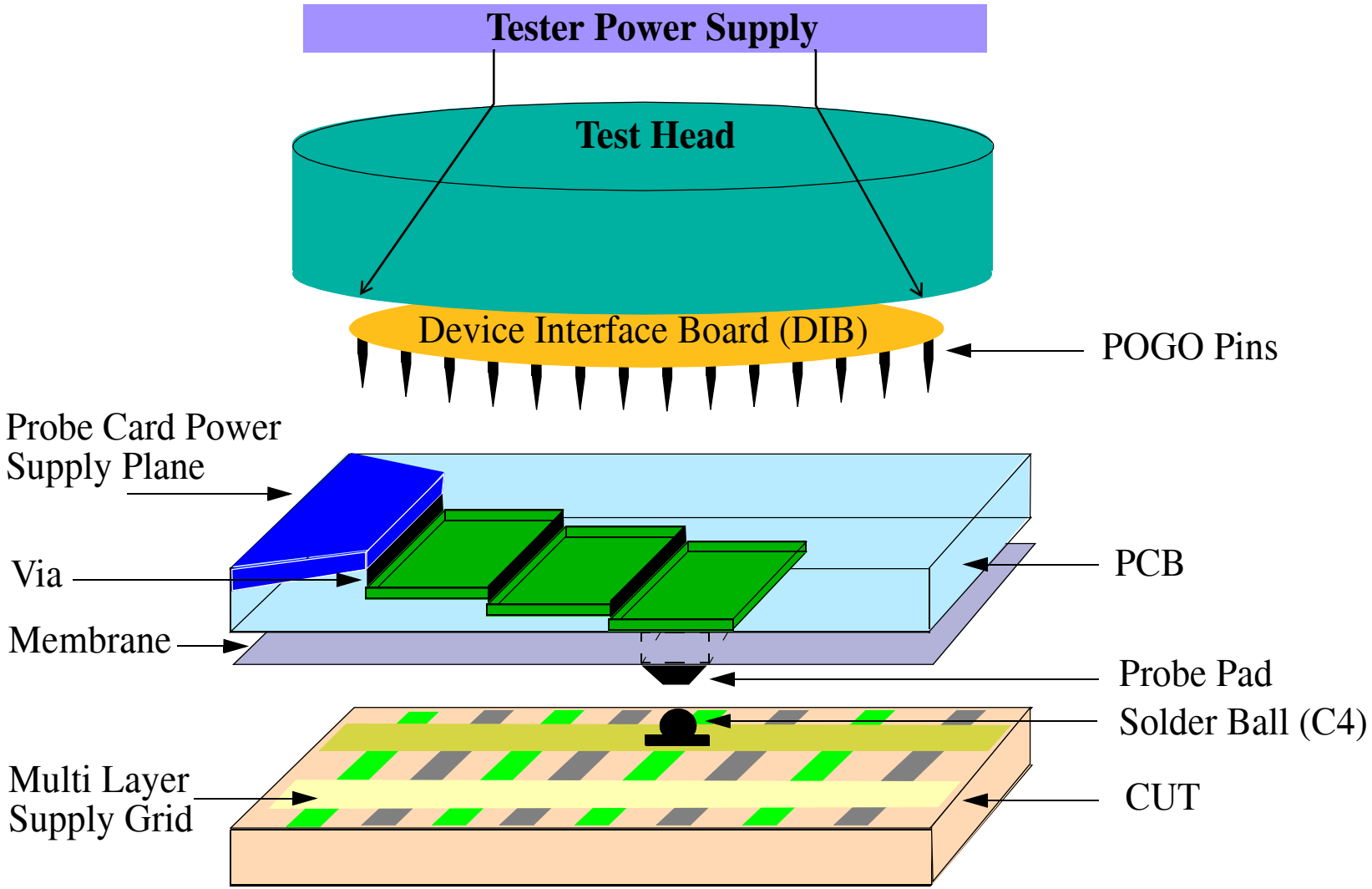
### *Frame processor*

Synchronizes the CUT input stimuli (from pattern generators) with sample-and-compare.

***Strobe time*** is interval between application of inputs and sampling of outputs.

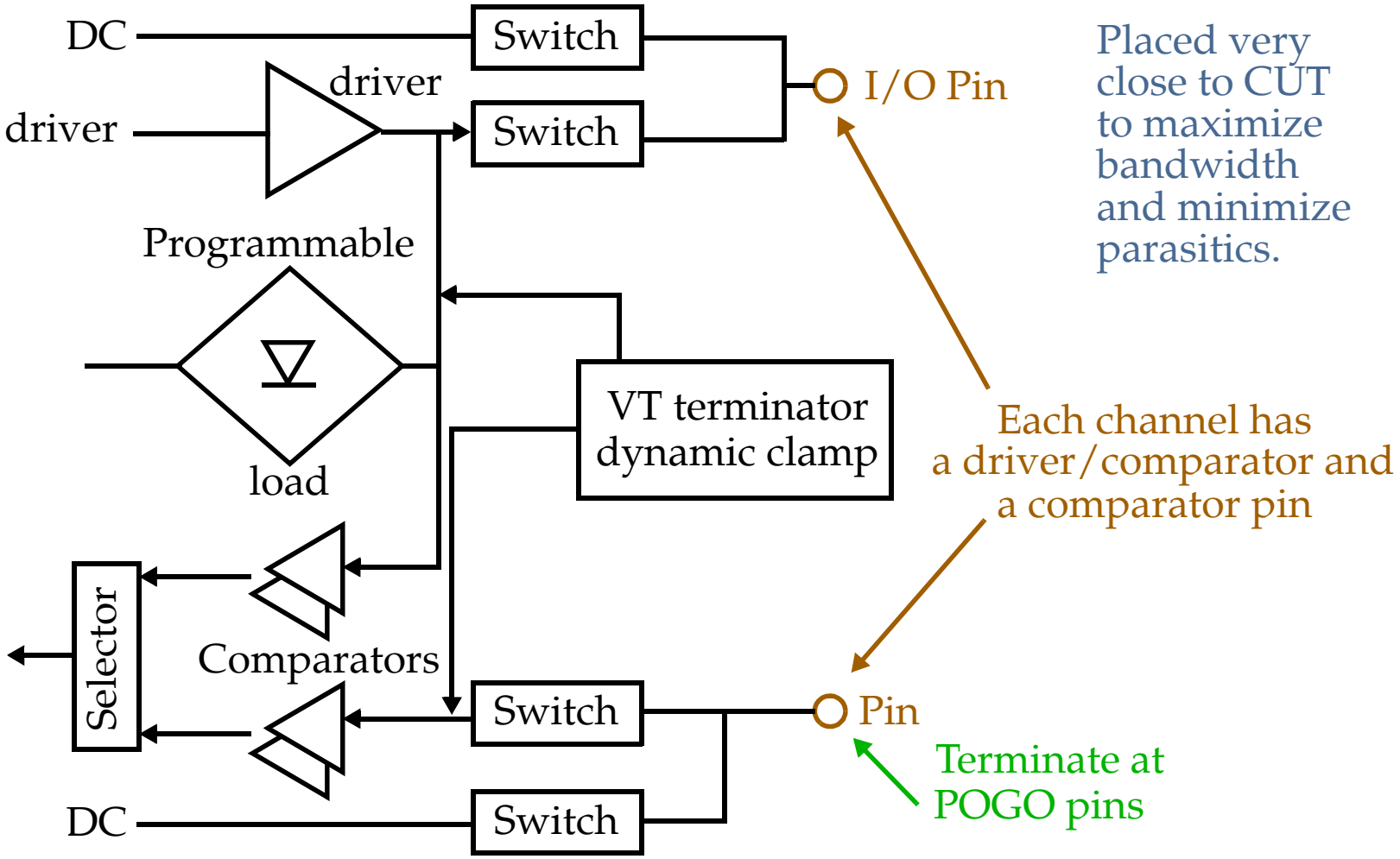
## *Test Head, Membrane Probe Card and CUT*

Test head and membrane (cobra) probe card for probing C4s.



## *Probing*

Pin electronics (PE) of Advantest T6682:



## *Probing*

***Wafer probe:*** POGO pins interface to Device Interface Board (DIB) and then a probe card.

***Package test:*** POGO pins interface with a package handler and then to a testing socket. (contactor)

***Pins/Channels:*** ATE has between 128 and 1024 pins, expandable in units of 128.

***Voltage Settings:*** $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $I_H$, $I_L$, $V_T$ (logic threshold voltage) and both dynamic clamp voltages for each channel can be independently set.

***Parametric measuring unit***

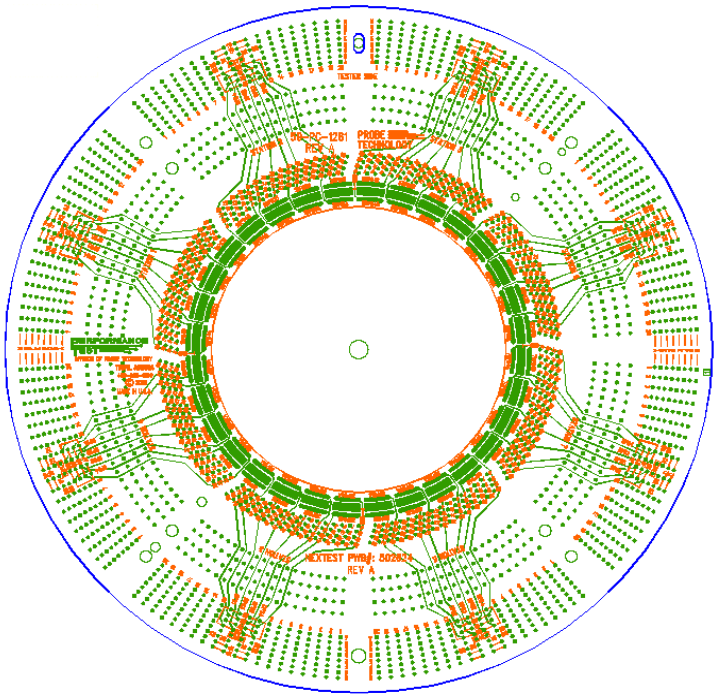
Applies and measures voltages or currents at a pin.

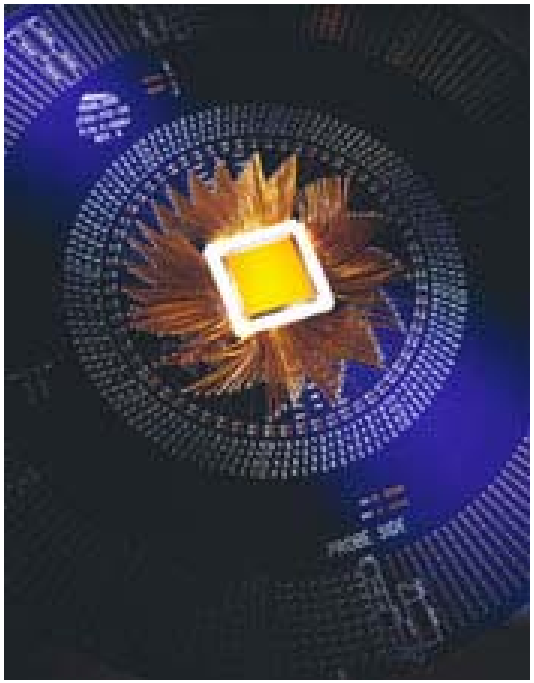
Two units are available: Multi-DC unit (MDC) and universal DC unit (UDC).

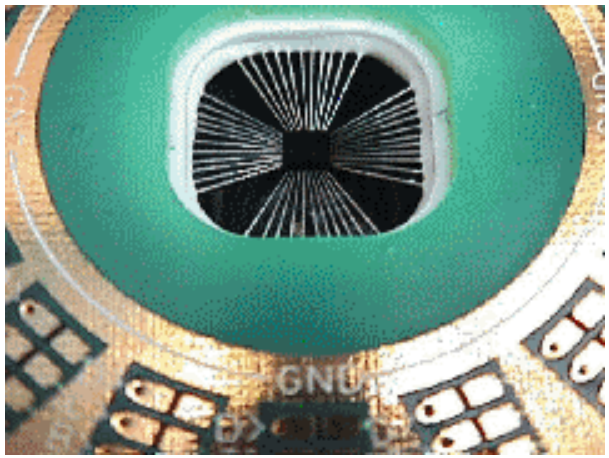
***Mixed-signal test***

ATE has additional components including a waveform generator, a digitizer, digital waveform capture memory, sine wave generator, etc.

## *Cantilever Style Probe Cards*







## *Other ATE Equipment*

24-32 power supplies.

OS is usually a unix variety, Solaris.

Solaris on one processor with non-real time functions.

Real-time OS on a second processor for tester control.

***Test Description Language*** **(TDL)** used to write test programs.

Can specify strobe times, voltage/current stimuli, vector application rate, vector slew rate, etc.

ATE software can:

- Generate a fail bit map for testing a memory chip.
- Generate a wafer map showing passing, failing and binning results of chips.
- Emulate a logic analyzer for debugging.
- Emulate an oscilloscope for capturing analog waveforms with high resolution.
- Generate schmoo plots.

## *Multi-Site Testing*

One ATE can test several (usually identical) devices at the same time.

Can be done at wafer probe or package test.

Motivation: Most of the cost is for the basic ATE.

Adding additional instruments is relatively inexpensive.

Digital and mixed signal: Usually can test 2 to 4 chips at time.

Memory chips frequently tested 32 and 64 at a time because the test times are very long.