The VLSI Testing Process

Verification testing, characterization testing and design debug:

    Verifies correctness of design and test procedure.

    More common to correct design than test procedure.
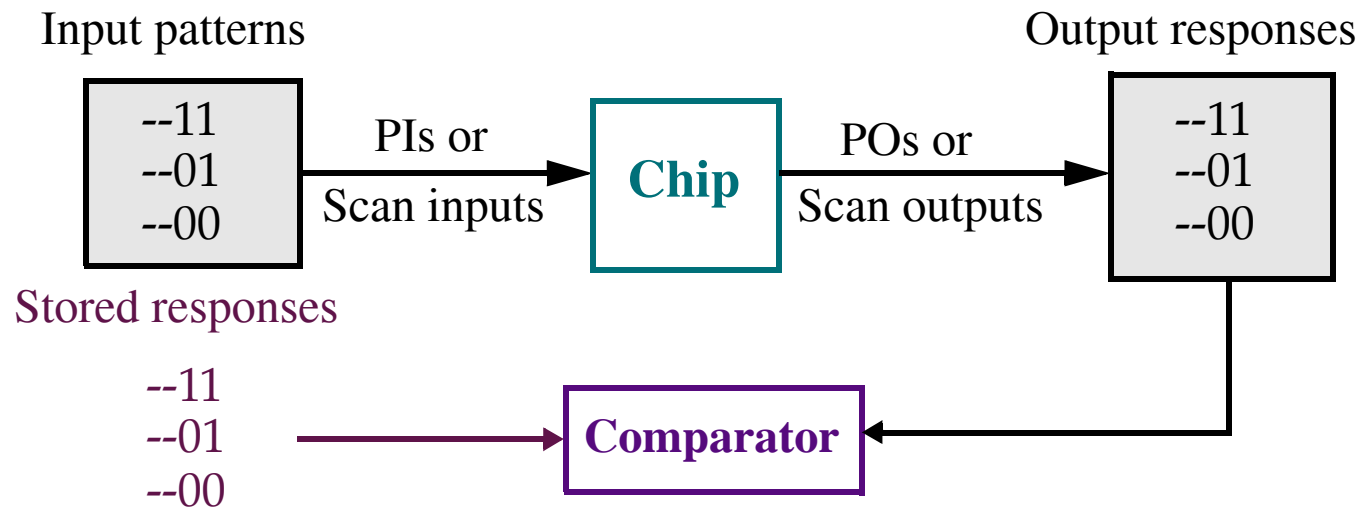
Manufacturing testing:

    Factory testing of all manufactured chips for parametric faults and for random defects.

Acceptance testing (incoming inspection):

    Customer performs tests on purchased parts to ensure quality.

Testing Principle

Input patterns

| --11 |
| --01 |
| --00 |

PIs or
Scan inputs

Chip

POs or
Scan outputs

Output responses

| --11 |
| --01 |
| --00 |

Stored responses

--11
--01
--00

Comparator

When the chip is digital, the stimuli are called **test patterns** or **test vectors**.

Automatic test equipment (ATE) carries out this process.

A powerful computer operating under the control of a **test program**, a program written in a high level language.

Digital signal processor (DSP) used for analog testing.

Chips are automatically fed to the tester through the wafer handler system.

A **probe card** or **membrane probe** contacts pads of bare or packaged chip.

Types of Testing

Verification testing

Performed on new designs -- determines if design is correct and meets specifications - - very expensive.

AC, DC and functional tests performed.
Probing of internal chip nodes may also be performed.
Functional tests maybe repeated multiple times.

Specialized tools are used, such as scanning electron microscopes (SEM) and electron beam tests.
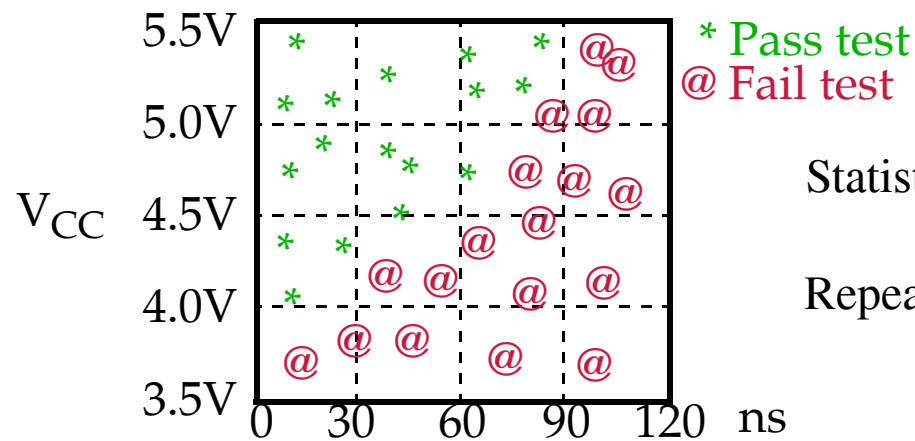AI and expect systems may also be useful.

Types of Testing

Characterization testing

Focus on tests that pass/fail chips

Focus on worst case corners -- shmoo plots are created

Helps in setting specification limits for production testing

V_{CC}

5.5V, 5.0V, 4.5V, 4.0V, 3.5V

0   30   60   90   120   ns

* Pass test
@ Fail test

Statistically significant number of chips are chosen

Repeated for all 2+ environment variables

Diagnose and correct design errors

Less intensive characterization test performed during normal life-cycle of chip
to improve design and process yield

Types of Testing

Manufacturing testing

This type of testing is referred as go/no-go testing

Determines if all the chips manufactured meet the specifications

Test should cover high percentage of modeled faults

No fault diagnosis, only an outgoing inspection test

Test at speed of application or speed guaranteed by the supplier

The main concern is cost as the tests need to be performed on each chip:

Must minimize test time

Tests need to be less extensive but optimized to give expected quality.

Types of Testing

Burn-in Testing

Subject chips to high temperature and elevated voltages, while running entire or sub-sets of production tests.

Some chips that pass production test will fail very quickly thereafter.
Burn-in ensures reliability by forcing failure in these "weak" chips.

They are responsible for screening:

Infant mortality failures: Often caused by a combination of sensitive design and process variation -- short-term burn-in effective (10-30 hours).

Freak failures: Same failure mechanism as reliable devices -- long-term burn-in required (100-1000 hours) -- very expensive.

Types of Testing

Incoming Inspection

Can be:

Similar to production testing
More comprehensive than production testing
Tuned to specific systems application

Often done for a random sample of devices

Sample size depends on device quality and system reliability requirements

Avoids putting defective devices in a system where cost of diagnosis exceeds incoming inspection cost

Types of Tests

Wafer sort or probe test:

Performed before wafer is scribed (cut into chips).

Test site characterization is also performed during wafer sort.
  Test structures are tested to characterize the technology including gate threshold,
    poly sheet resistance, etc.

Packaged device tests

Sub-types of tests include:

Parametric tests:

DC parametric tests include shorts test, opens test, leakage test, etc.
AC parametric tests include delay test, setup and hold test, etc.

Functional Tests:

Test every transistor and wire.
Designed to cover a high % of modeled faults -- long and expensive.

Types of Tests

Functional Tests (contd.):

The test vectors used for verifying that the chip meets specs are called functional vectors.

Typically they have low fault coverage (<70%).

Functional vectors targeting manufacturing defects usually have higher coverage.

We'll distinguish functional patterns, when we introduce structural test patterns.

Functional test may be applied at elevated temperature to guarantee specifications.

They can also be used to "speed bin" parts.

Accomplished by applying the tests at different voltages and varying the clock frequency.

Types of Tests
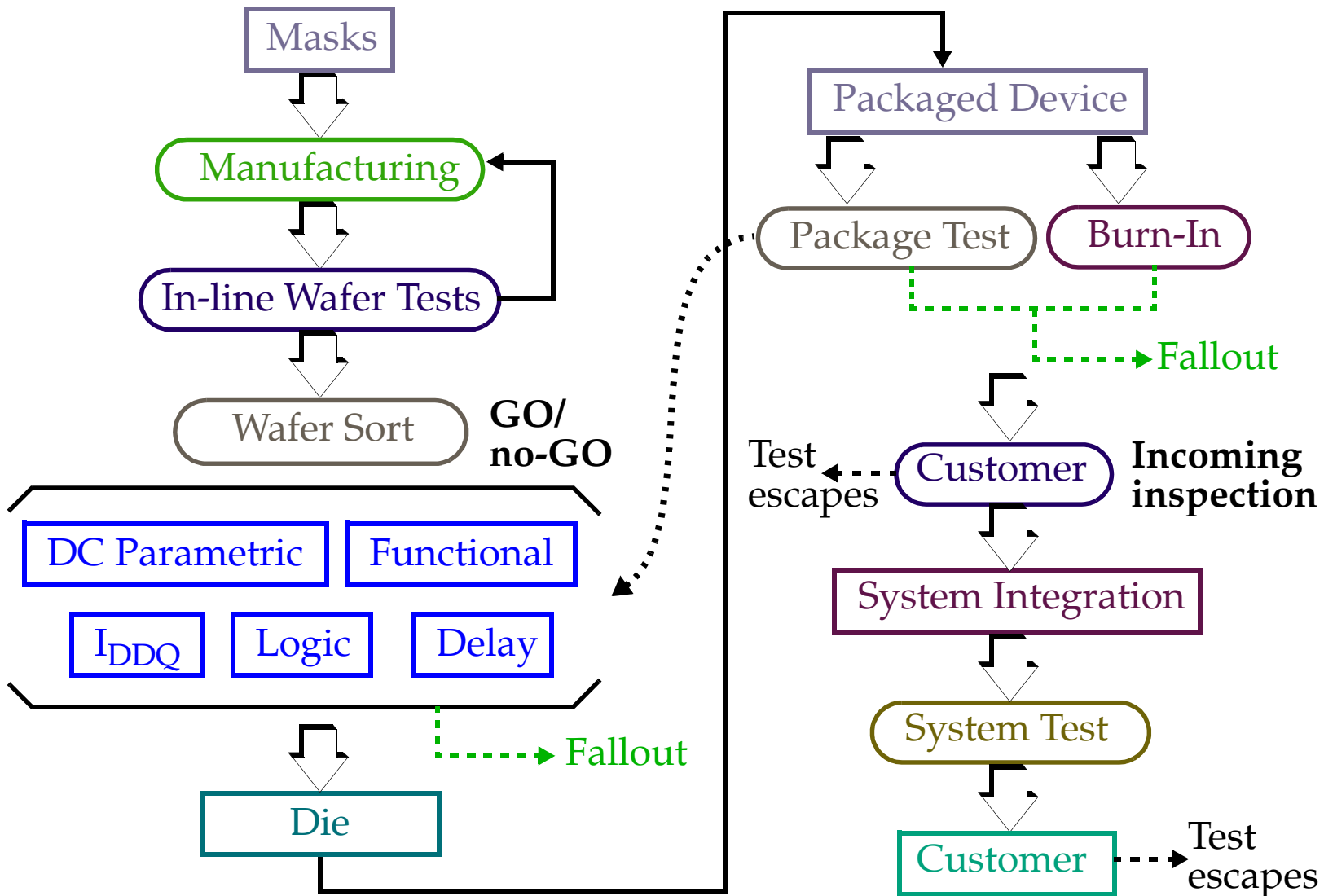
Test Specifications and Test Plan

The chip specification document initiates test development.

It contains:
- Functional characteristics, e.g. algorithm to be implemented, I/O signal characteristics (timing and signal levels), clock rate.
- Type of chip, e.g., microprocessor, memory, mixed-signal, etc.
- Physical characteristics, e.g., pin assignments, etc.
- Technology, e.g., gate array, custom, std cell, etc.
- Environmental characteristics, e.g., operating temperature, supply voltage, etc.
- Reliability, e.g., acceptance quality level (defects per million, dpm), failure rate per 1,000 hours, noise characteristics.
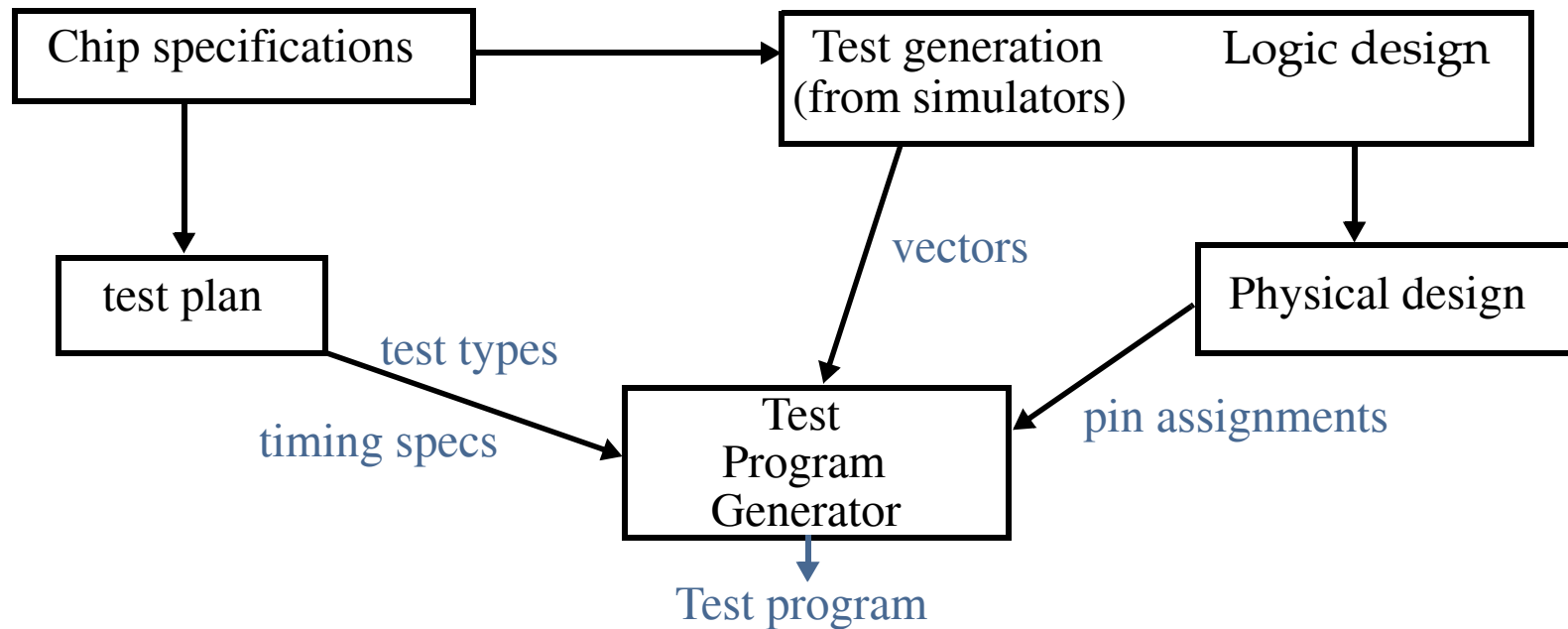
These are used to derive a test plan, which includes
- Type of test equipment to use, i.e., required clock rate, timing accuracy, etc.
- Types of tests.
- Fault coverage requirements.

Test Programming

The test program, the digital test vectors and the analog test waveforms are needed once the chip is mounted in the tester.

CAD tools to automate the generation of the test programs.

```
┌─────────────────────┐                    ┌──────────────────────────────────────┐
│ Chip specifications │ ─────────────────► │ Test generation      Logic design    │
└─────────────────────┘                    │ (from simulators)                    │
          │                                └──────────────────────────────────────┘
          │                                         │                    │
          ▼                                         │ vectors            ▼
┌──────────────┐                                    │           ┌──────────────────┐
│  test plan   │                                    │           │  Physical design │
└──────────────┘                                    │           └──────────────────┘
          │      test types                         ▼                    │
          │                              ┌────────────────────┐          │
   timing specs                          │        Test        │ pin assignments
          └────────────────────────────► │      Program       │ ◄────────┘
                                         │     Generator      │
                                         └────────────────────┘
                                                   │
                                                   ▼
                                             Test program
```

3 main purposes of the ATE test data:

• Accept/reject the chip-under-test (CUT).

• Provides information about the fabrication process (via FA).

• Provides information about design weaknesses (via FA).