VLSI Design Verification and Testing

Instructor

Chintan Patel

(Contact using email: cpatel2@cs.umbc.edu).

Text

Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing, for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers (2000).

Supplementary texts

Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design," Revised, IEEE Press (1990).

Samiha Mourad and Yervant Zorian, "Principles of Testing Electronic Systems", Wiley (2000).

Further Info

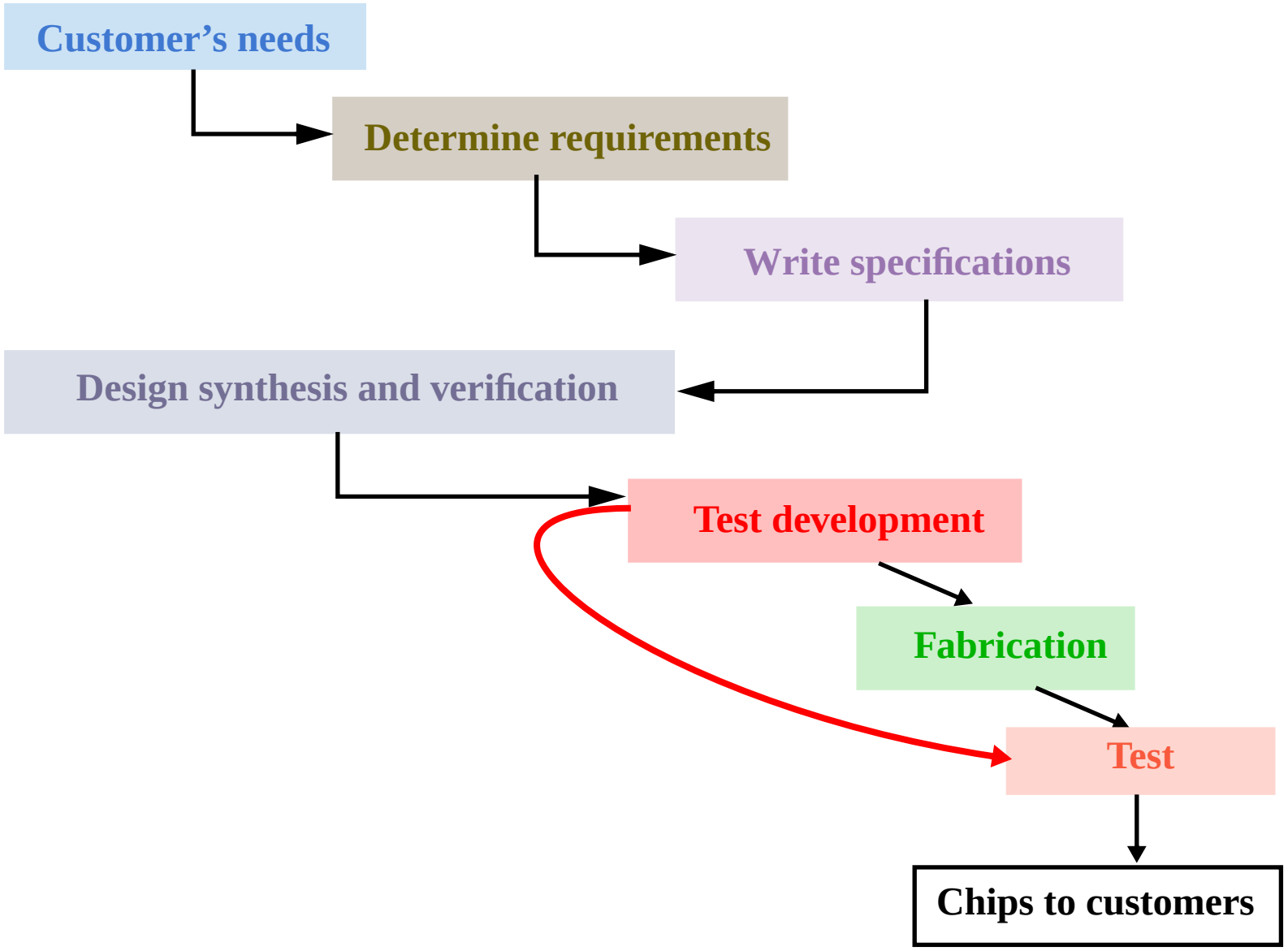
http://www.cs.umbc.edu/~cpatel2

Purpose of the Course

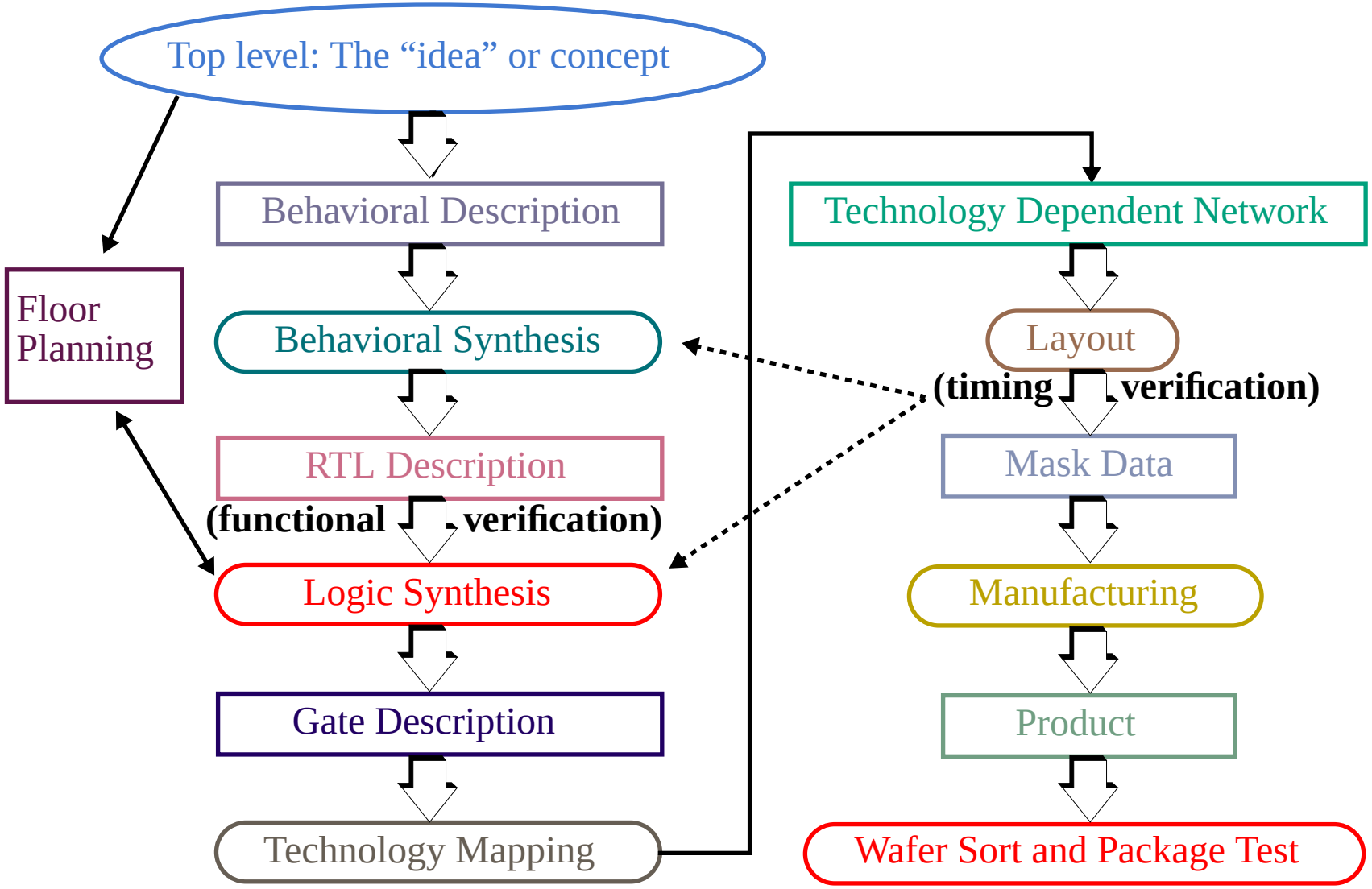
To introduce the concepts and techniques of design verification and manufacturing test of digital integrated circuits.

- Only an overview of design verification is covered.
- Design verification will eventually be covered in a course of its own.
- Major focus of this course will be on device testing.

VLSI Design and Test Process



VLSI Design and Test Flow



Important Terms/ Definitions

- ***Design Synthesis:*** Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- ***Verification:*** Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- ***Test:*** A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Design Verification vs. Testing

Verification

* Verifies correctness of design.
* Performed by simulation, hardware emulation or formal methods.
* Performed "once" prior to manufacturing.

Test

* Verifies correctness of hardware.
* Two-parts:
  - Test generation: software process executed "once" during design.
  - Test application: electrical tests applied to hardware.
* Test application performed on EVERY manufactured device.

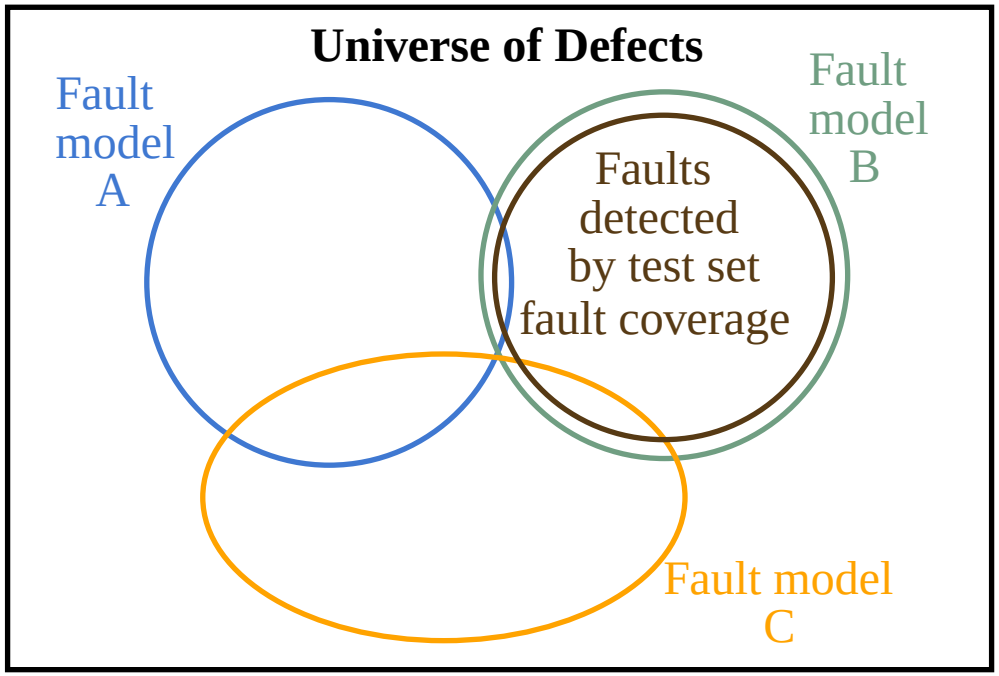
Ideal vs Real Tests

- Ideal tests detect all defects produced in a manufacturing process.
  Pass all functionally good chips, fail all defective chips.

- Very large numbers and varieties of possible defects need to be tested.

- Difficult to generate tests for some real defects. ***Defect-Based Testing (DBT)*** is a HOT research area.

Ideal tests can detect all defects in this universe



Ideal vs Real Tests

Real Test are based on analyzable fault models which may not map to real defects

A ***fault*** is a logic level abstraction of a ***physical defect*** that is used to describe the change in the logic function of a device caused by the defect.

It is difficult to generate tests that detect every possible fault in the chip due to high design complexity.

Some good chips are rejected.

The fraction of such chips is called ***yield loss***.

Some bad chips are shipped.

The fraction of bad chips among all passing chips is called ***defect level (test escapes)***.

Benefits of Testing:

Quality and economy: Quality means satisfying the user's need at a minimum cost.

VLSI Technology Trends and Imapct on Testing

Year	97-01	03-06	09-12
Feature size (μm)	0.25-0.15	0.13-0.10	0.07-0.05
Millions of transistors/cm^2	4-10	18-39	84-180
Number of wiring layers	6-7	7-8	8-9
Die size, mm^2	50-385	60-520	70-750
Pin count	100-900	160-1475	260-2690
Clock rate, MHz	200-730	530-1100	840-1830
Voltage, V	1.2-2.5	0.9-1.5	0.5-0.9
Power, W	1.2-61	2-96	2.8-109

These trends impact cost and difficulty of testing

- Rising Chip Clock Rates (exponential trend)

At-Speed Testing

Experiments suggest stuck-at tests more effective when applied at-speed.

This requires at-speed testers.

VLSI Technology Trends and Imapct on Testing

Automated Test Equipment (ATE) Cost

Example from text:

State-of-the-art ATE can apply tests >250 MHz.

Purchase price of a 500MHz tester: $1.2M + (1,024 pins * $3,000/pin) = $4.272M.

Running cost: Depreciation + Maintenance (2%) + Operating cost = $0.85M + $0.085M + $0.5M = $1.439M/year.

Testing cost for round-the-clock operation: $1.439M/(365 * 24 * 3,600) = 4.5 cents/second.

Digital ASIC test time = 6 seconds or 27 cents.

For a yield of 65%, test component of sale price is 27/0.65 = 41.5 cents.

VLSI Technology Trends and Imapct on Testing

- Increasing Transistor Density

  Feature size reduces by ~10.5%/year leading to density increase of ~22.1%/year.

  Wafer and chip size increases in combination with process innovations double this to ~44%/year.

  This indicates that # of transistors double every 18 to 24 months (Moore's Law).

Test Complexity

Increasing transistor density impacts testing as test complexity increases due to access restrictions.

In the worst case, computational time for test pattern generation increases exponentially with # of PIs and on-chip FFs.

VLSI Technology Trends and Imapct on Testing

For example: Consider a square chip with width = d.

# of transistors, N_t, on the chip is proportional to the area, d^2.

# of peripheral I/O pins, N_p, is proportional to 4d.

Rent's rule is given by:

$$N_p = K\sqrt{N_t}$$

Therefore, the test procedure must access a larger number of gates through a proportionately smaller number of pins.

A rough measure of test complexity can be expressed as N_t/N_p.

For example, the 97-01 roadmap data indicates 107/900 = 11,000.

VLSI Technology Trends and Imapct on Testing

Power Dissipation

Another impact on testing due to increase in transistor density

$$\textbf{Power density} = C \times V_{DD}^2 \times f$$

Constant electric field (CE) scaling keeps the power density constant.

$$C \rightarrow \alpha C \qquad V_{DD} \rightarrow \frac{V_{DD}}{\alpha} \qquad f \rightarrow \alpha f$$

CE scaling not practical in submicron region since switching speed decreases as V_{DD} approaches threshold voltage.Therefore, supply voltage scaled by

$$\frac{\varepsilon}{\alpha} \quad \textbf{with} \quad \varepsilon > 1$$

and power density increases by

$$\varepsilon^2$$

Testing must check for power grid IR drop and application of the tests must consider power dissipation.

Reducing threshold voltage increases leakage (I_{DDQ} problems).

Costs of Testing

Design for Testability (DFT):

Chip area overhead

Yield reduction

Performance penalty

Software processes of test:

Test generation

Fault simulation

Test programming and debug

Manufacturing test:

Automatic test equipment (ATE) capital cost

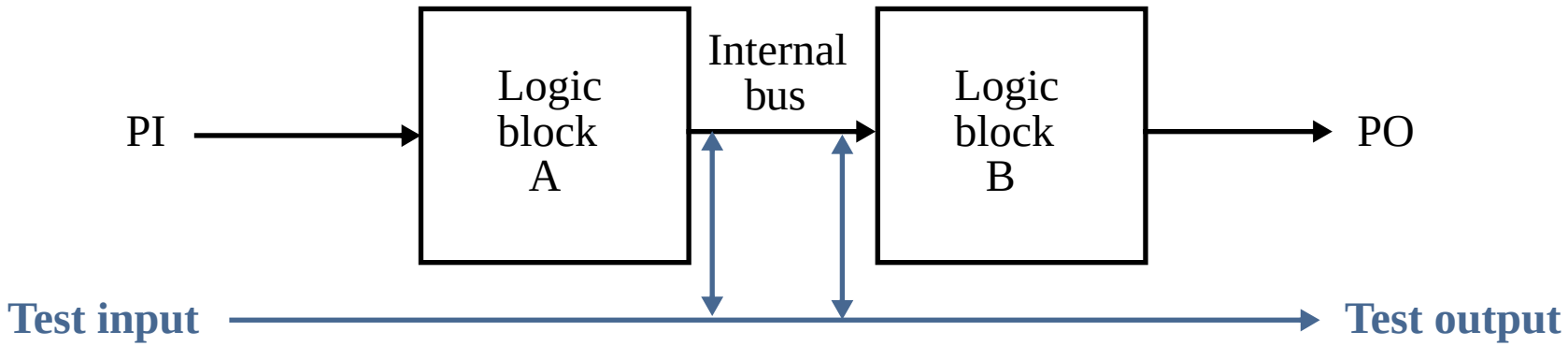
Test center operational cost

Design for Testability (DFT)

DFT refers to hardware design styles or added hardware that reduces test generation complexity and test application cost.

As indicated before, test generation complexity increases exponentially with size of the chip.

A simple example of simplifying the test generation process:



Roles of Testing

Detection: Go/no-go, is the chip fault-free or faulty.

Must be fast.

Diagnosis: Determine where the failure occurred in the chip and what caused it.

Performed on some chips that fail go/no-go tests.

Device characterization: Determination and correction of error in design and/or test procedure.

Failure Analysis (FA): Determination of manufacturing process errors that may have caused defects on the chip.

Topics to be covered

We will attempt to cover the following topics as time permits:

- Basic concepts and definitions
- Test process and ATE
- Test Economics
- Faults
- Fault Simulation
- Testability Measures
- ATPG
- Different Testing Methods (I_{DDQ}, Delay etc.)
- Scan design
- BIST (Built in Self Test)
- Boundary Scan
- Other advanced topics