CMPE 414/CMPE 641: Advanced VLSI Design

Course:

CMPE 414/ CMPE 641: Advanced VLSI Design.
Sections 0101.
Spring 2005. 3 credits.

Course Instructor:

Chintan Patel, Research Asst. Prof., Computer Science & Electrical Engineering
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Office Hours: M&W 11:00-12:30pm or by appointment
Teaching Assistants: Abhishek Singh
TA Office Hours: TBA.

Text:

Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis", Second Edition, Kluwer Academic Publishers (2002)

Supplementary texts:

David Smith and Paul Franzon, "Verilog Styles for Synthesis of Digital Systems", Prentice Hall (2000).
Dirk Janser et al., "The Electronic Design Automation Handbook", Kluwer Academic Publishers (2003).
Sachin Sapatnekar, "Timing", Kluwer Academic Publishers (2004).
Farzad Nekoogar, "Timing Verification", Prentice Hall (1999).
Cadence online documentation (cdsdoc)
Synopsys online documentation (SOLD)

Course Description:

This course introduces automated design tools, required for netlist synthesis, place & route and timing verification. Other advanced topics related to the design automation flow will be covered as time permits. Students will design a standard cell library for their project. Tools from both Synopsys Inc. and Cadence Design Systems will be introduced in this course.

Grading:

The distribution of weights is as follows:

Standard Cell Library Development	20%
Project coding	20%
Project Implementation	40%
Exam (optional). Grade will be distributed evenly between above categories, if no exam is given.	20%

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No incompletes will be given, except as required by university policy for truly exceptional circumstances.

NOTE: Cheating at any time in this course will cause you to fail the course.

By enrolling in this course, each student assumes the responsibilities of an active participant in UMBC's scholarly community in which everyone's academic work and behavior are held to the highest standards of honesty. Cheating, fabrication, plagiarism, and helping others to commit these acts are all forms of academic dishonesty, and they are wrong. Academic misconduct could result in disciplinary action that may include, but is not limited to, suspension or dismissal. To read the full Student Academic Conduct Policy, consult the UMBC Student Handbook, the Faculty Handbook, or the UMBC Policies section of the UMBC Directory [or for graduate courses, the Graduate School website].

The following is taken from the UMBC Student Handbook:

DEFINITIONS OF ACADEMIC MISCONDUCT

Academic misconduct may include but is not limited to the following:

Cheating: knowingly using or attempting to use unauthorized material, information, or study aids in any academic exercise.

Fabrication: Intentional and unauthorized falsification or invention of any information or citation in an academic exercise.

Facilitating Academic Dishonesty: Intentionally or knowingly helping or attempting to help another commit an act of academic dishonesty.

Plagiarism: Knowingly representing the words or ideas of another as one's own in any academic exercise, including works of art and computer-generated information/images.

POLICY FOR RESOLVING CASES OF ACADEMIC MISCONDUCT

Individual faculty members have the right and responsibility to deal directly with any cases of academic misconduct which arise in their courses. Instances of academic misconduct may be identified in one of two ways. If a faculty member believes a student has committed an act of academic misconduct--for example, by direct observation of student behavior, by comparing the contents of an assignment with that submitted by another student, or by reviewing notated sources or references--the faculty member, in consultation with the Chair of the Academic Conduct Committee, will assess the student's alleged misconduct and the faculty member's options. If a student believes that academic misconduct has occurred, the student will notify either the faculty member or the Chair of the Academic Conduct Committee.

It is particularly important that the Chair of the Academic Conduct Committee be consulted. The Chair can provide knowledge and insight for the faculty member. Communication of instances of academic misconduct also protects the integrity of the university by providing a means of recording infractions that may be repeated by a particular student, or which may prove endemic to a particular course or department. Consultation with the Chair of the Academic Conduct Committee provides a formal record of the infraction and resolution, protecting the student, professor, and university should any questions later arise.

The student will have the opportunity to respond to an accusation of academic misconduct.

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Tentative Course Outline

Topics	Timeline
Standard Cell Library Development Topics include: Layout (GDS II), Abstract Generation (LEF), Verilog, Circuit Extraction (Space), Circuit Simulation (Spice, TLF), Timing arcs and constraints, IO cells.	3 classes Assignment: 3 weeks
Verilog Synthesizable verilog, basic constructs, simulators, test benches, combination and sequential constructs, state machines, datapath elements, FIFOs, multiple clock domain design.	6 classes Assignment: 4 weeks
Synthesis, Place & Route Synthesis tools, synthesis techniques, timing verification, floorplanning, power grid design, clock insertion, scan insertion, place & route.	Remainder of classes Assignments: Remainder of classes

Note: Changes/Additions to this schedule will be posted on my website
http://www.cs.umbc.edu/~cpatel2/