Standard Cell Libraries

Standard cell libraries are required by almost all CAD tools for chip design

Standard cell libraries contain primitive cells required for digital design

However, more complex cells that have been specially optimized can also be included

The main purpose of the CAD tools is to implement the so called RTL-to-GDS flow

The input to the design process, in most cases, is the circuit description at the register-transfer level (RTL)

The final output from the design process is the full chip layout, mostly in the GDSII (gds2) format

To produce a functionally correct design that meets all the specifications and constraints, requires a combination of different tools in the design flows

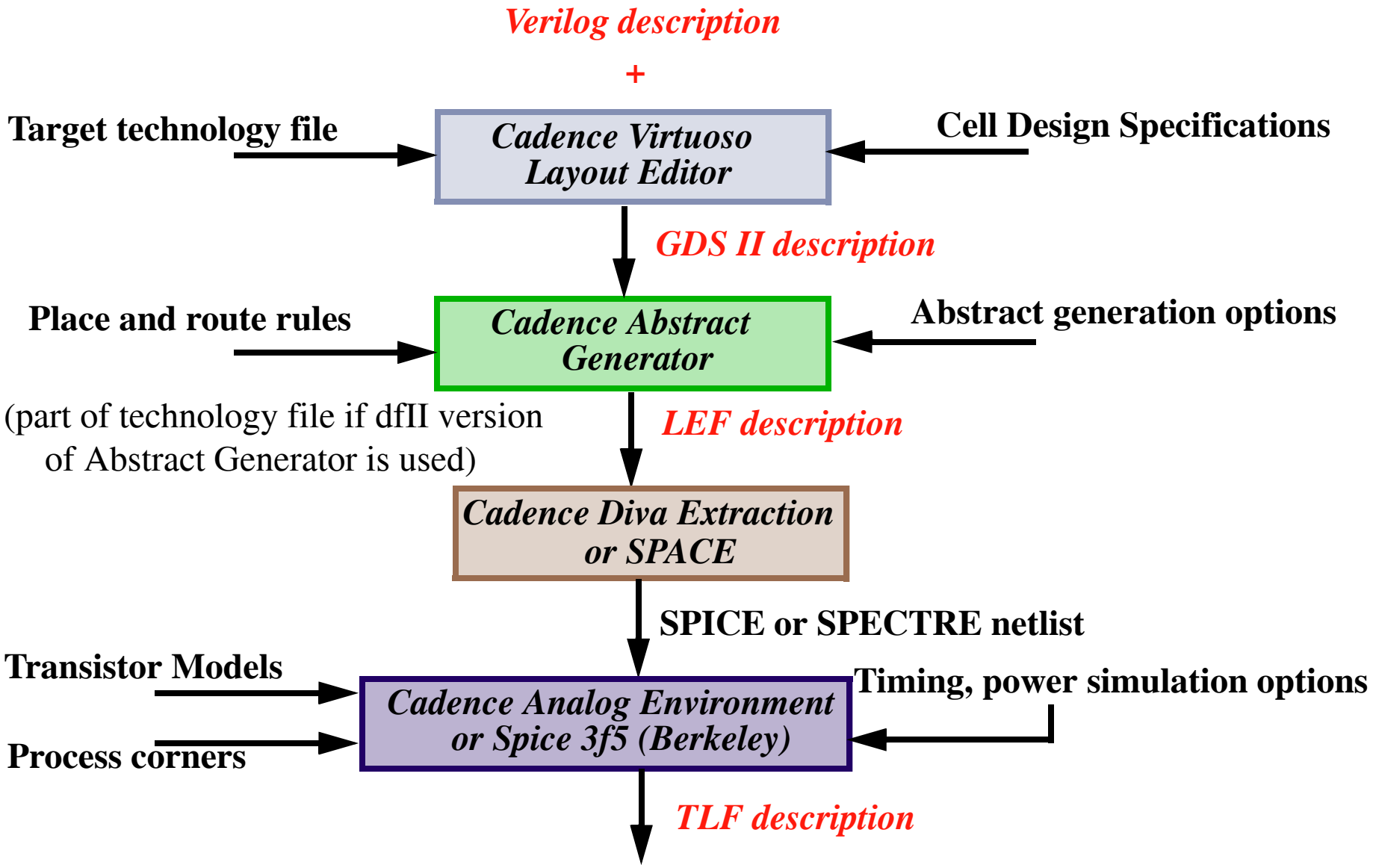
These tools require specific information in different formats for each of the cells in the standard cell library provided to them for the design

Standard Cell Library Formats

The formats explained here are for Cadence tools, howerver similar information is required for other tool suites.

- Physical Layout (gdsII, Virtuoso Layout Editor)
  - Should follow specific design standards eg. constant height, offsets etc.
- Logical View (verilog description or TLF)
  - Verilog is required for dynamic simulation. Place and route tools usually can use TLF.
  - Verilog description should preferably support back annotation of timing information.
- Abstract View (Cadence Abstract Generator, LEF)
  - LEF: Contains information about each cell as well as technology information
- Timing, power and parasitics (TLF)
  - Transistor and interconnect parasitics are extracted using Cadence or other extraction tools (SPACE).
  - Spice or Spectre netlist is generated and detailed timing simulations are performed.
  - Power information can also be generated during these simulations.
  - Data is formatted into a TLF file including process, temperature and supply voltage variations.
  - Logical information for each cell is also contained in the TLF file.

Standard Cell Library Formats



Standard Cell Layout

Routing Grids

Both vertical and horizontal routing grids need to be defined

HVH or VHV routing is defined for alternating metals layers

All standard cell pins must be placed on intersection of horizontal and vertical routing grids
- Exceptions are abutment type pins (VDD and GND)

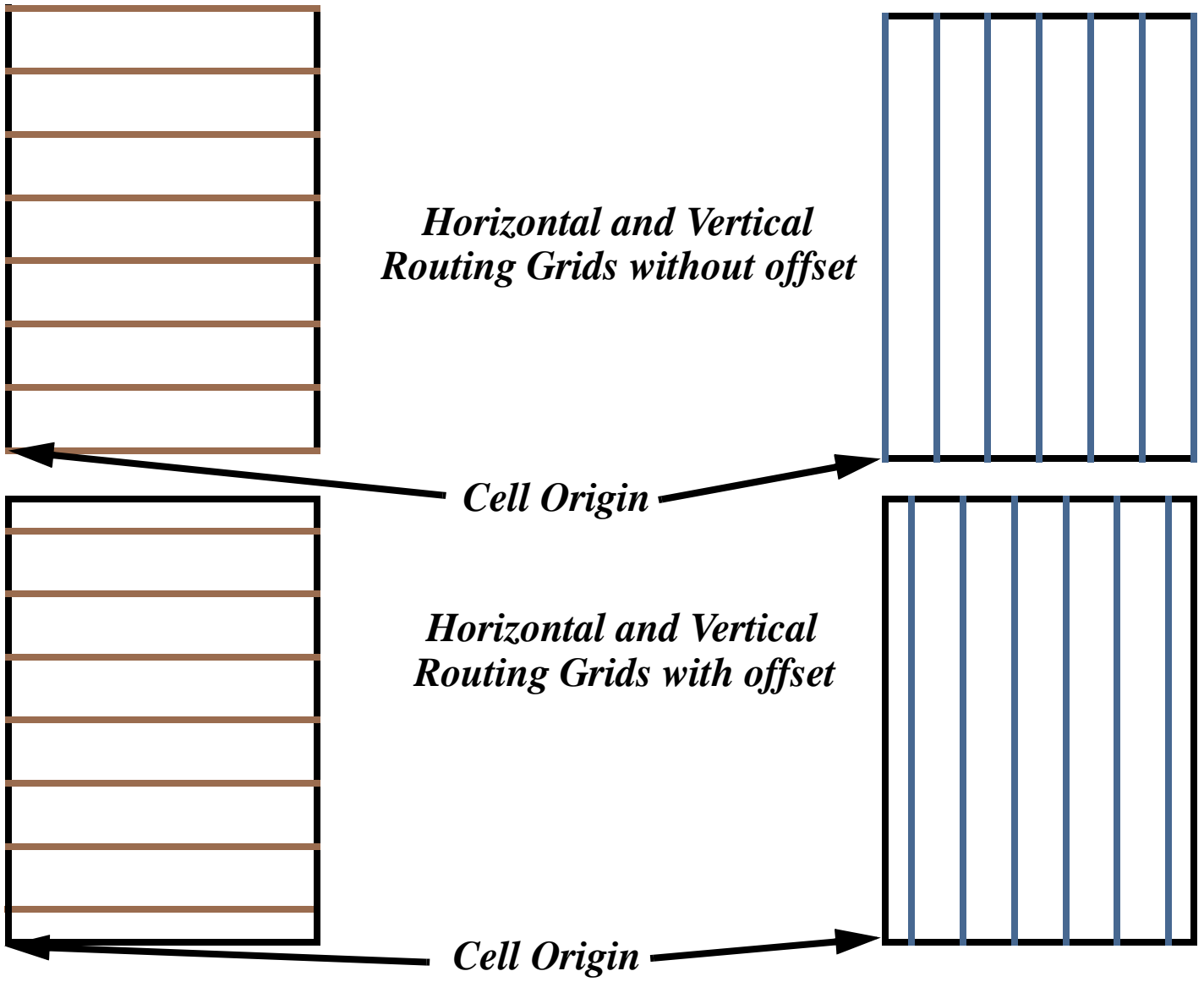
Grids are defined wrt the cell origin

Grids can be offset from the origin, however by exactly half the grid spacing

The cell height must be a multiple of the horizontal grid spacing
- All cells must have the same height, but some complex cells can be designed with double height

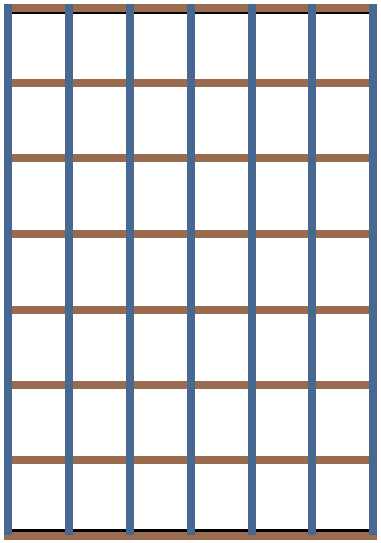
The cell width must be a multiple of the vertical grid spacing
- However, limited routing tracks are the bottleneck even with wider cells

Standard Cell Layout

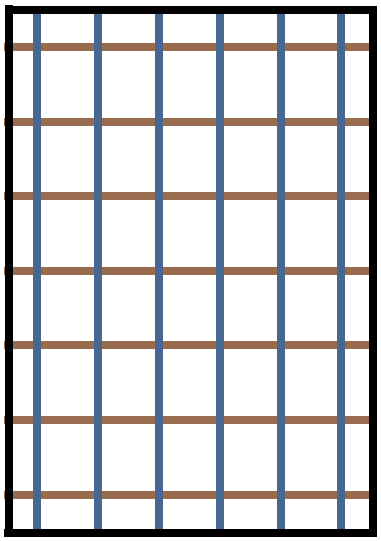


Standard Cell Layout

Routing Grids without offset



Routing Grids with offset

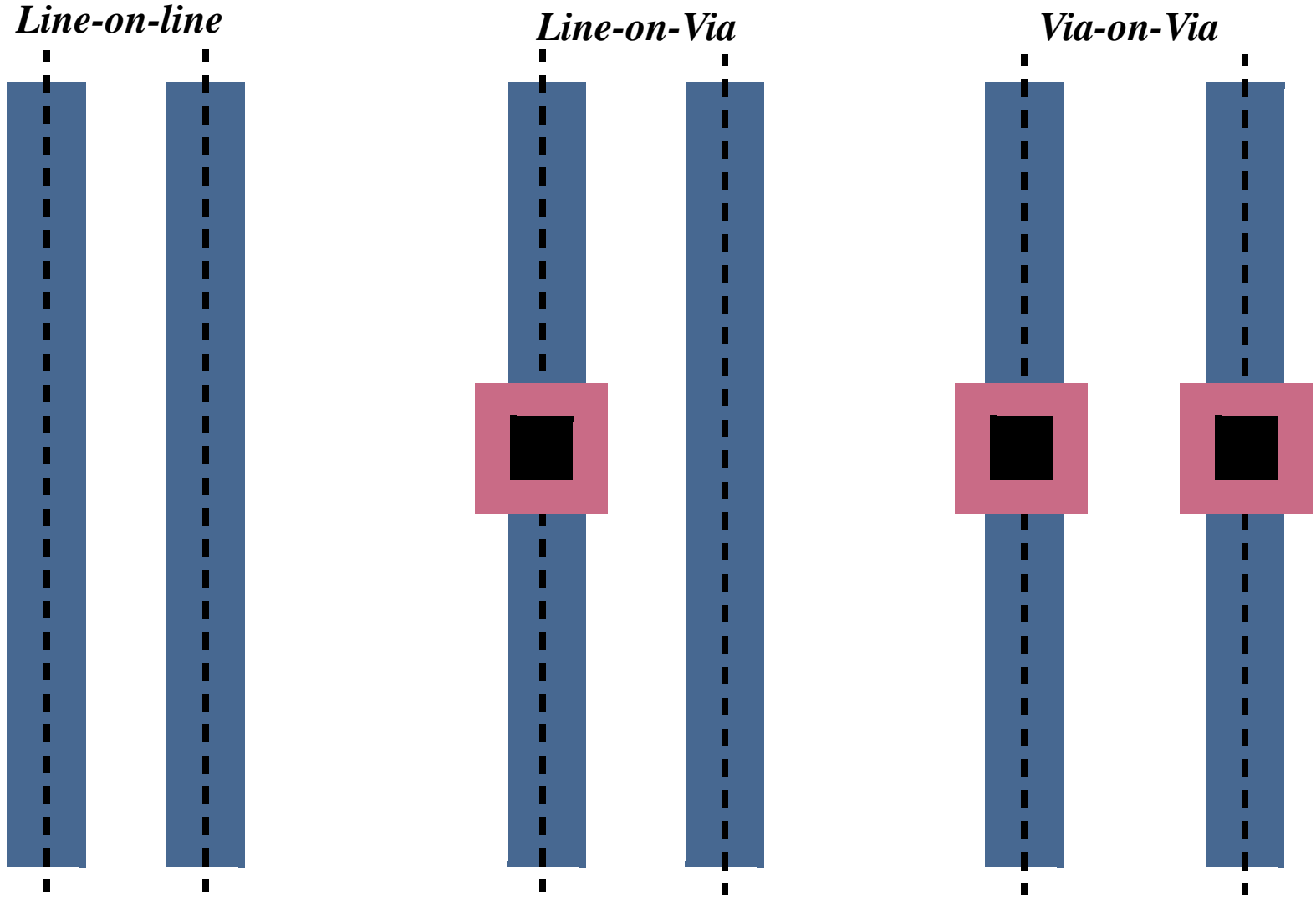


Routing grids are used by the CAD tools to route wires over the standard cells placed in the design

Some CAD tools can route off grid, however most are optimal when they route on grid

Standard Cell Layout

Routing Grid Spacing



UMBC Standard Cell Library

AMI 0.6 μm technology

- NCSU design kit provides the basic technology file for the process
- Enhanced with custom place and route rules added here

Horizontal grid spacing: 3.0 μm or 10λ

- Offset is 1.5 μm or 5λ

Vertical grid spacing: 2.4 μm or 8λ

- Offset is 1.2 μm or 4λ

Horizontal routing layers: Metal1 and Metal3

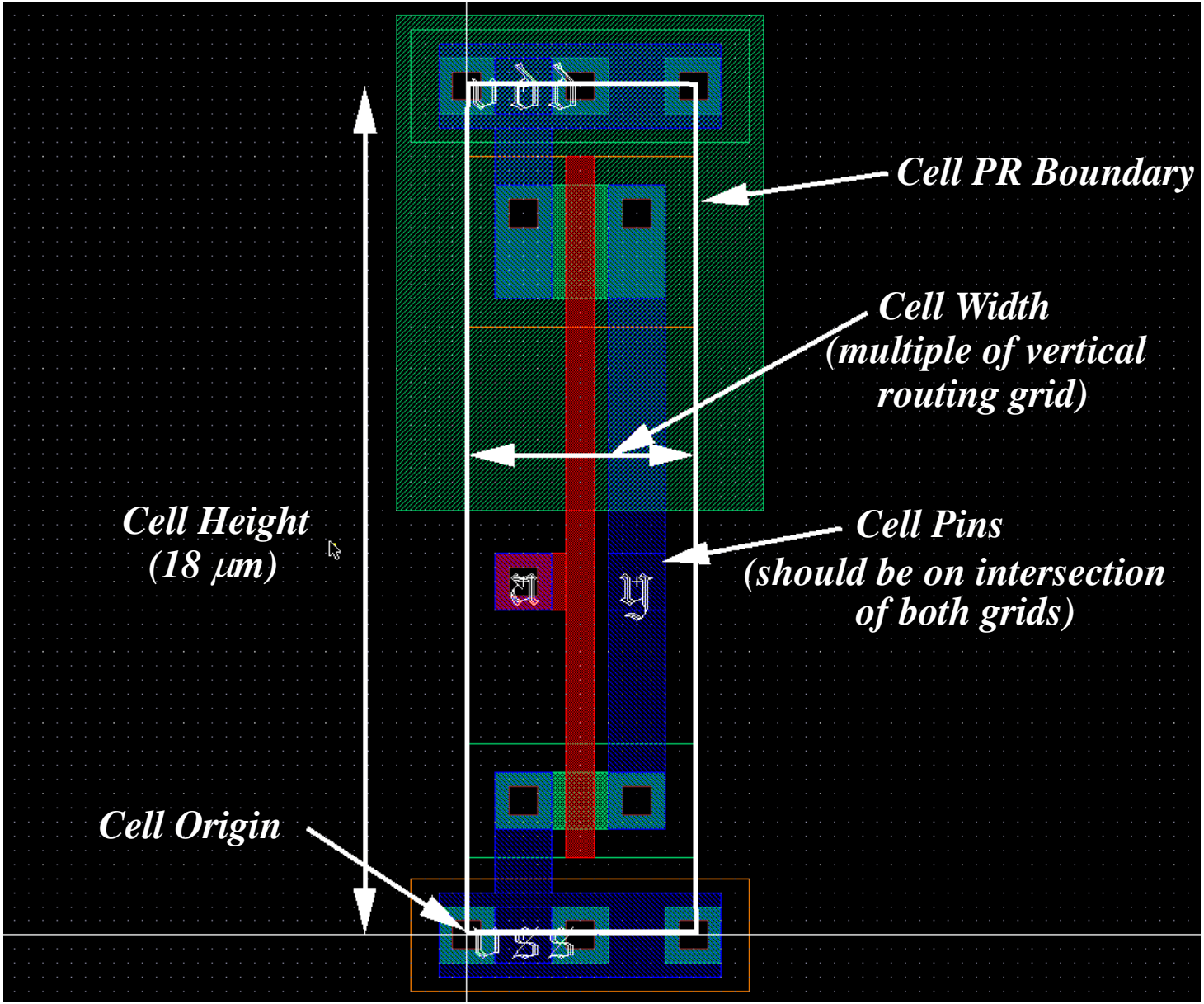
Vertical routing layers: Metal2

Cell height: 18 μm or 60λ. VDD and GND rail width: 1.8 μm or 6λ

Half the cell height for N and P transistors i.e. n-well boundary ends at half the cell height

Size P transistors to provide approximately same performance as the N transistors

Inverter (invx1) Standard Cell Layout



NAND (nand2x4) Standard Cell Layout