CMPE 414/641: Assignment 6

Verilog Design (Due: Mon Mar 28)

Write a verilog description for the following ALU circuit:

Input A: 4-bits 2’s complement
Input B: 4-bits 2’s complement
Output Y: 4-bits 2’s complement
Control: 2-bit input

Your design should perform the following operations:

Control Input	Operation Performed
00	Y=A+B
01	Y=A-B
10	Y= A shift right arithmetic by amount given by 2 least significant bits of B
11	Y= A shift left by amount given by 2 least significant bits of B

Write the verilog description in all the three following levels of abstraction:

(1) Behavioral
(2) Data-Flow
(3) Structural

Write a test-bench to test your design. A single test-bench should be able to simulate all three descriptions of your design.