CMPE 315: Principles of VLSI Design

Course:

CMPE 315: Principles of VLSI Design, Spring 2021. 4 credits.

Course Instructor:

Chintan Patel, Associate Professor, Computer Science & Electrical Engineering
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Office Hours: Tue - Thrs 4:00 - 5:30 PM or by appointment.
Teaching Assistants: (details will be posted on the class webpage)

Text:

Neil H.E. Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," Fourth Edition, Addison Wesley (2011)

Supplementary text:

Ken Martin, "Digital Integrated Circuit Design", Oxford University Press (2000).

Jan M. Rabaey, A. Chandrakasan, B. Nikolic "Digital Integrated Circuits, A Design Perspective", Second Edition, Prentice Hall (2003).

Grading:

The distribution of weights for the exams, homeworks and projects is as follows:

Exam	20%
Labs/Homework	35%
Project	40%
Class Participation, In-class exercise, Attendance.	5%

No incompletes will be given, except as required by university policy for truly exceptional circumstances.

The final exam is cumulative. However, material covered after the second exam will be emphasized.

Students are encouraged to participate in class.

NOTE: Cheating at any time in this course will cause you to fail the course.
Please refer to the guidelines on the next page.
For a complete description of academic dishonesty, refer to the UMBC Student Handbook.

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The following is taken from the UMBC Student Handbook:

DEFINITIONS OF ACADEMIC MISCONDUCT

Academic misconduct may include but is not limited to the following:

Cheating: knowingly using or attempting to use unauthorized material, information, or study aids in any academic exercise.

Fabrication: Intentional and unauthorized falsification or invention of any information or citation in an academic exercise.

Facilitating Academic Dishonesty: Intentionally or knowingly helping or attempting to help another commit an act of academic dishonesty.

Plagiarism: Knowingly representing the words or ideas of another as one's own in any academic exercise, including works of art and computer-generated information/images.

POLICY FOR RESOLVING CASES OF ACADEMIC MISCONDUCT

Individual faculty members have the right and responsibility to deal directly with any cases of academic misconduct which arise in their courses. Instances of academic misconduct may be identified in one of two ways. If a faculty member believes a student has committed an act of academic misconduct--for example, by direct observation of student behavior, by comparing the contents of an assignment with that submitted by another student, or by reviewing notated sources or references--the faculty member, in consultation with the Chair of the Academic Conduct Committee, will assess the student's alleged misconduct and the faculty member's options. If a student believes that academic misconduct has occurred, the student will notify either the faculty member or the Chair of the Academic Conduct Committee.

It is particularly important that the Chair of the Academic Conduct Committee be consulted. The Chair can provide knowledge and insight for the faculty member. Communication of instances of academic misconduct also protects the integrity of the university by providing a means of recording infractions that may be repeated by a particular student, or which may prove endemic to a particular course or department. Consultation with the Chair of the Academic Conduct Committee provides a formal record of the infraction and resolution, protecting the student, professor, and university should any questions later arise.

The student will have the opportunity to respond to an accusation of academic misconduct.

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Tentative Course Outline:

Week #	Topic
1	Introduction (Lab: Linux/CADENCE setup/tutorial)
1	Basic CMOS Logic Gate Design
2	Transformations: layout/schematic/Boolean expressions
2	CMOS Processing Technology (Lab 1: VHDL)
3	CMOS Processing Technology
3	CMOS Processing Technology
4	MOS Transistors(Lab 2: Schematics and Simulation using SpectreS)
4	MOS Transistors (Lab 3: Layout and Circuit Extraction)
5	MOS Transistors
5	MOS Transistor (Lab 4: Advanced Layout and Simulations)
6	MOS Transistors
6	Technology and Abstractions (Lab 5: Layout and LVS)
7	Midterm Exam (Date subject to change depending on material covered)
7	Exam Review/Performance Estimation (Lab: Project groups and discussion)
8	Performance Estimation (Lab: Project specification/VHDL)
8	Silicon Run I Movie
9	TBD (Lab: Project VHDL/Schematic)
9	CMOS Circuit and Logic Design
10	CMOS Circuit and Logic Design (Lab: Project Schematic/Layout)
10	CMOS Circuit and Logic Design
11	CMOS Circuit and Logic Design (Lab: Project Layout)
11	Advanced Topics
12	Advanced Topics
12	Advanced Topics
13	Advanced Topics (Lab: Project Simulations)
13	Advanced Topics
14	Advanced Topics (Lab: Final project reports, demos and presentations)
14	Final review
Final week	Final exam

(Note: Changes/Additions to this schedule will be posted on my web site http://www.cs.umbc.edu/~cpatel2/)