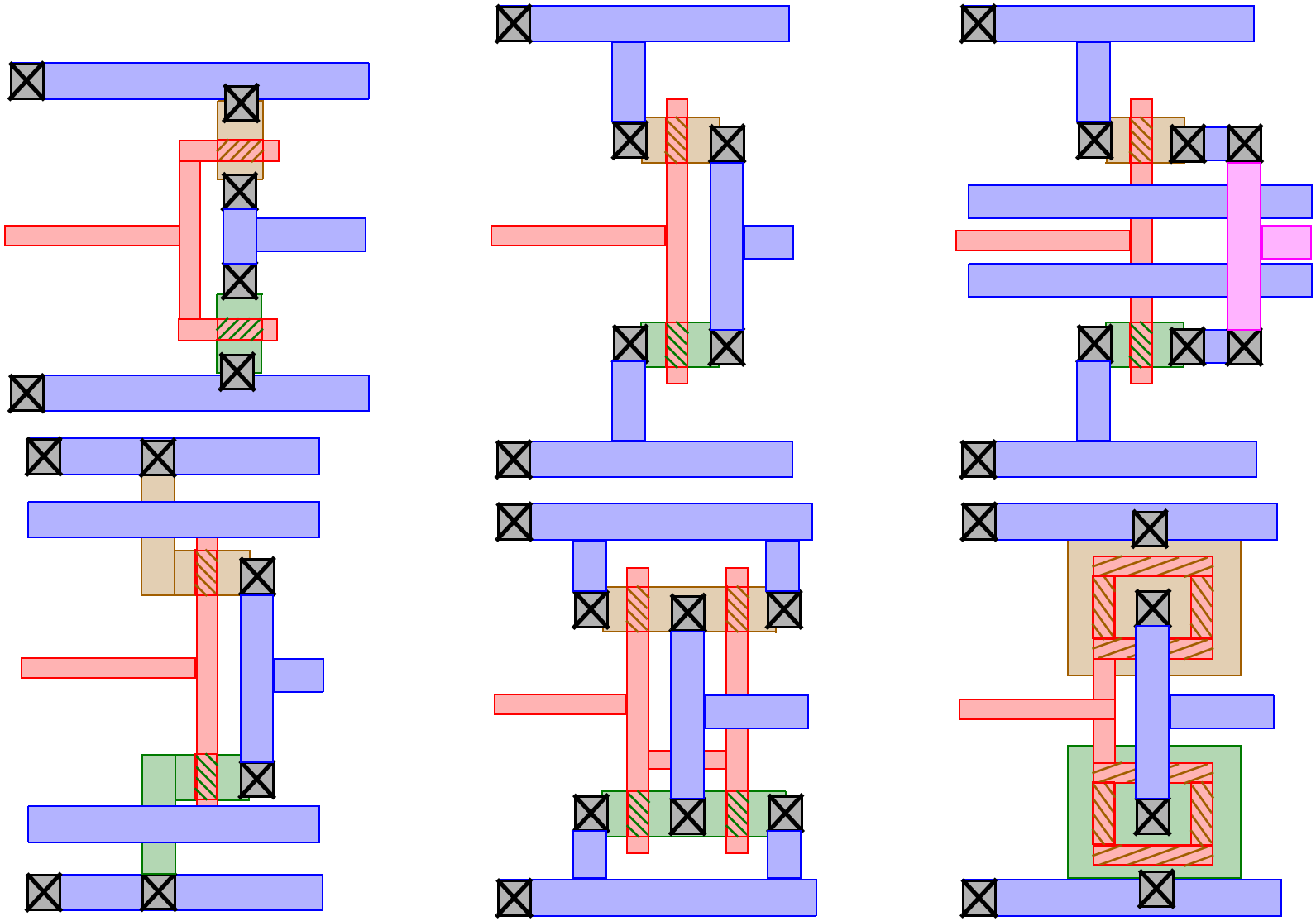
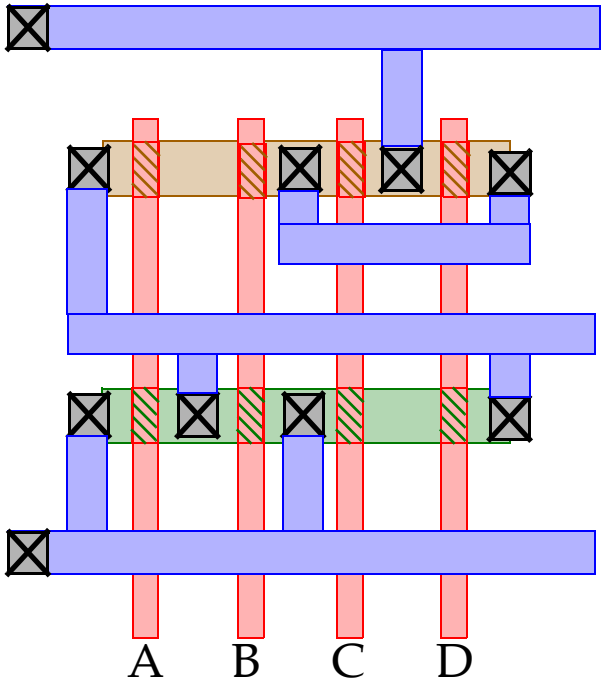
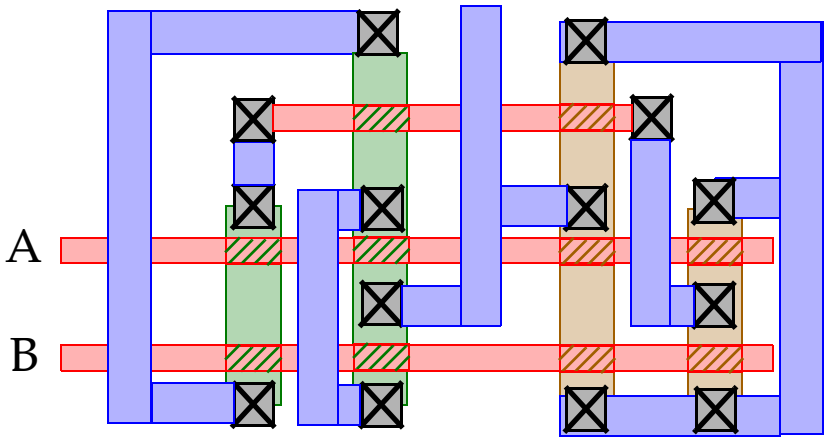
Inverter layout alternatives:



Complex Logic Gates



XNOR



Single unbroken line of diffusion not possible.

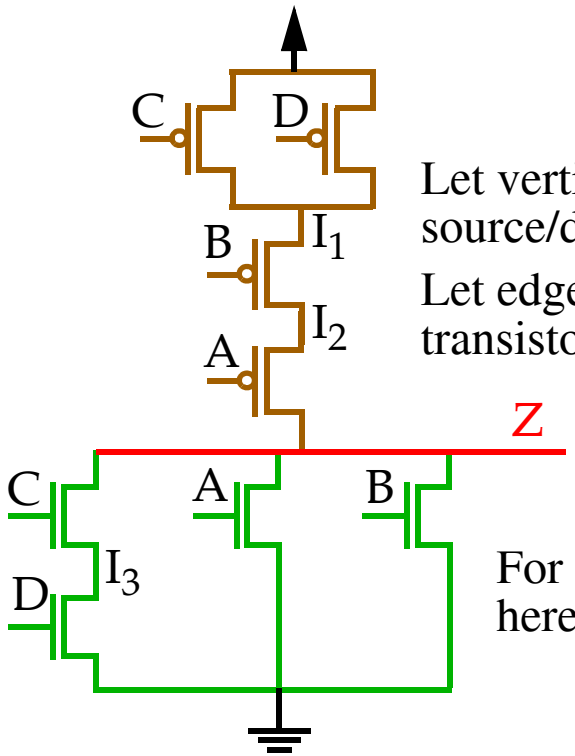
"Stacked layout" (on right): signals applied to multiple n- and p-transistors. Works well for cascaded gates.

Complex Logic Gates

Line of diffusion rule

Transistors form a line of diffusion intersected by poly.

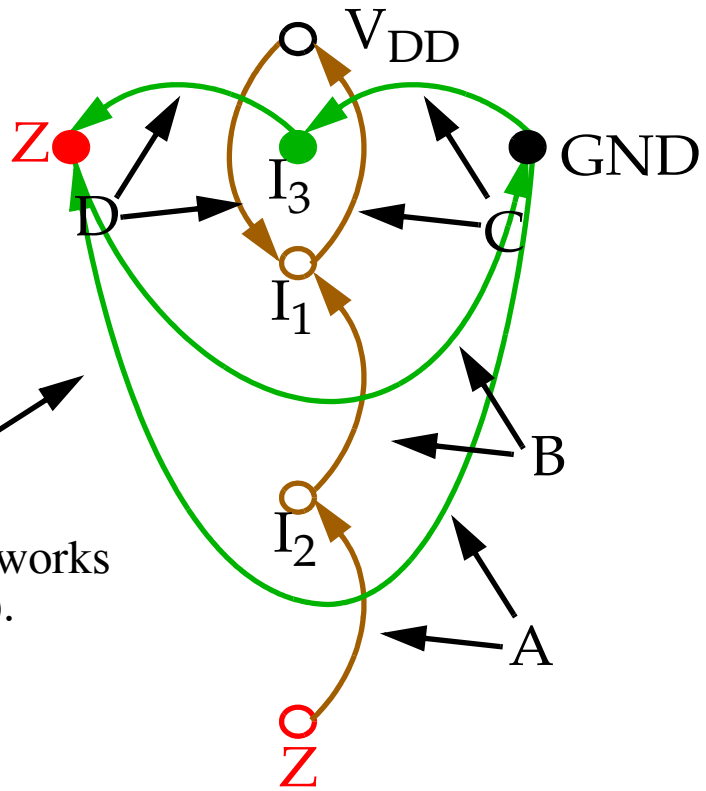
Diffusion will be unbroken if identically labeled Euler paths can be found for the p and n trees:



Let vertices represent source/drain connections.

Let edges represent transistors.

For example, A-B-C-D works here (see previous slide).



More Layout Examples

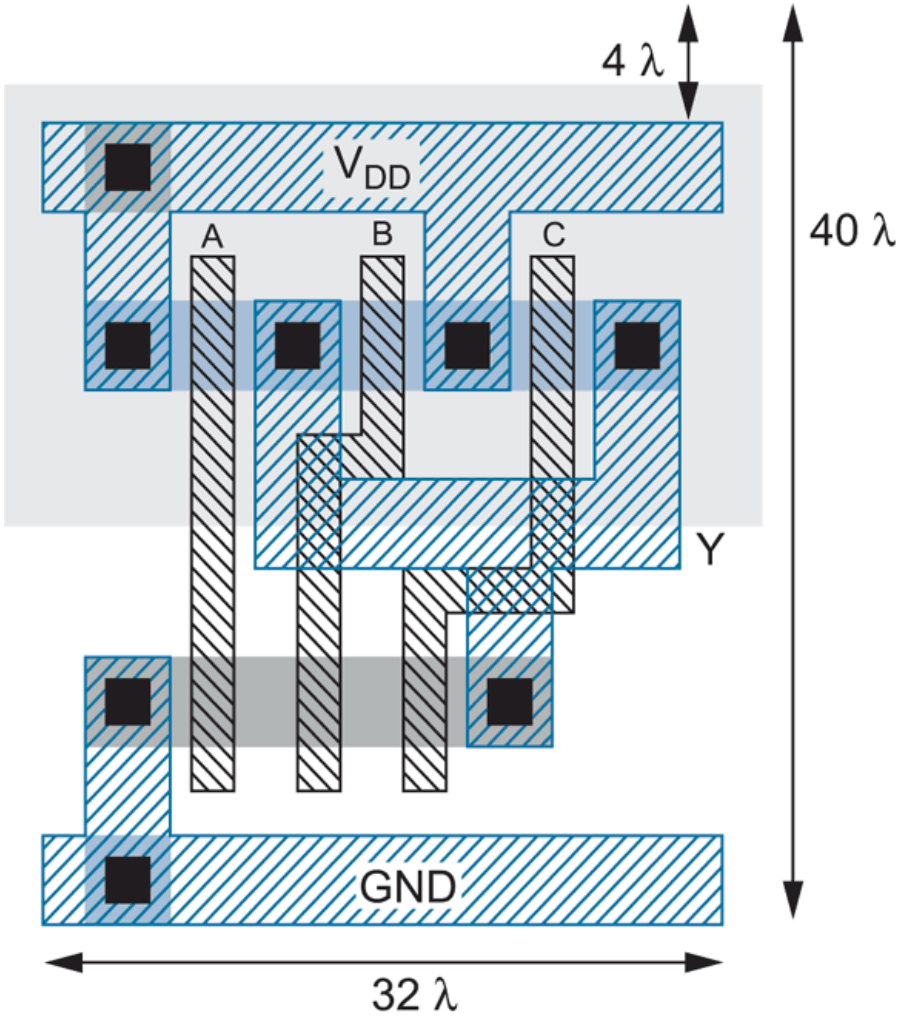


FIG 1.42 3-input NAND standard cell gate layouts

More Layout Examples

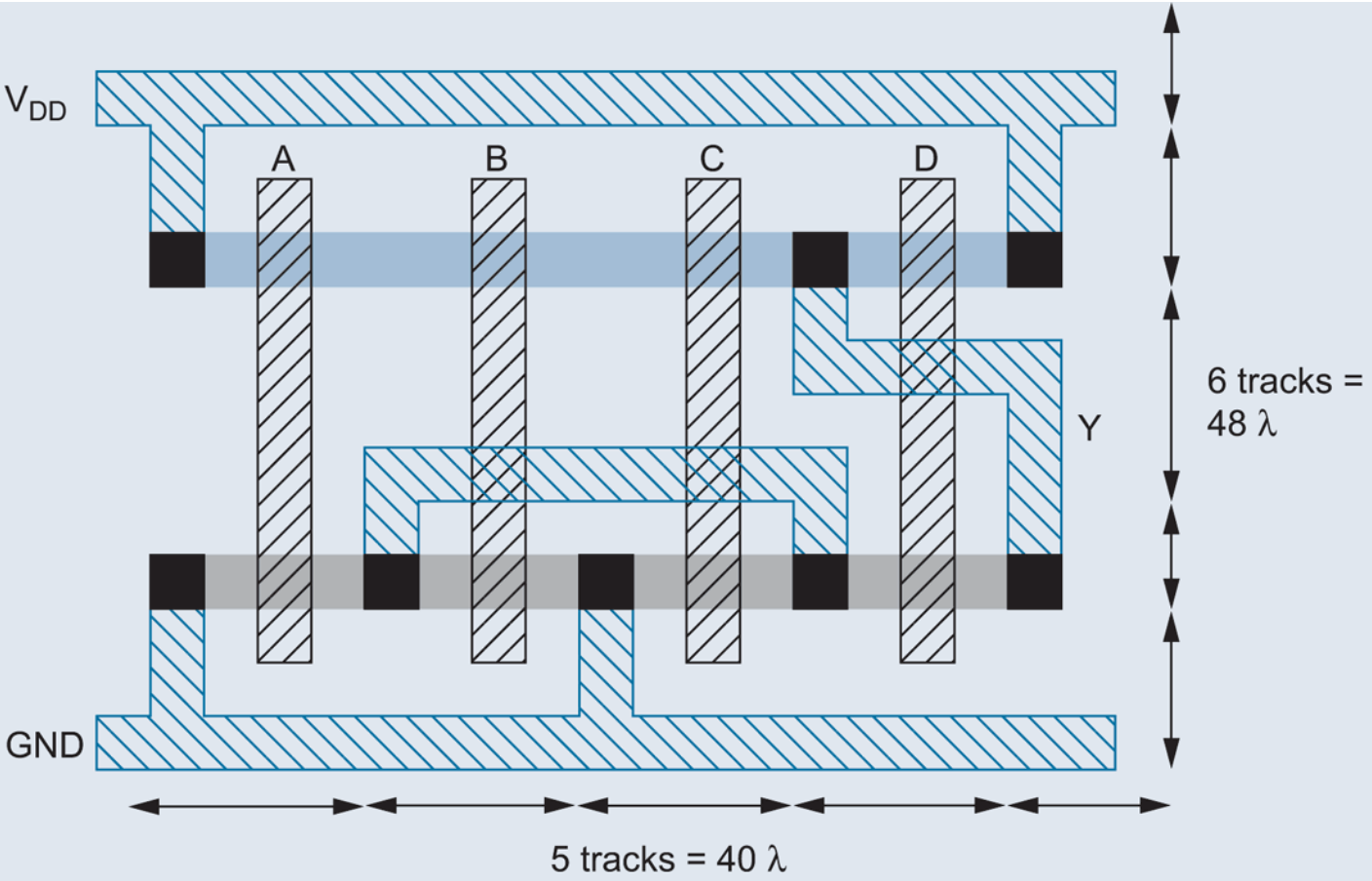


FIG 1.47 CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

More Layout Examples

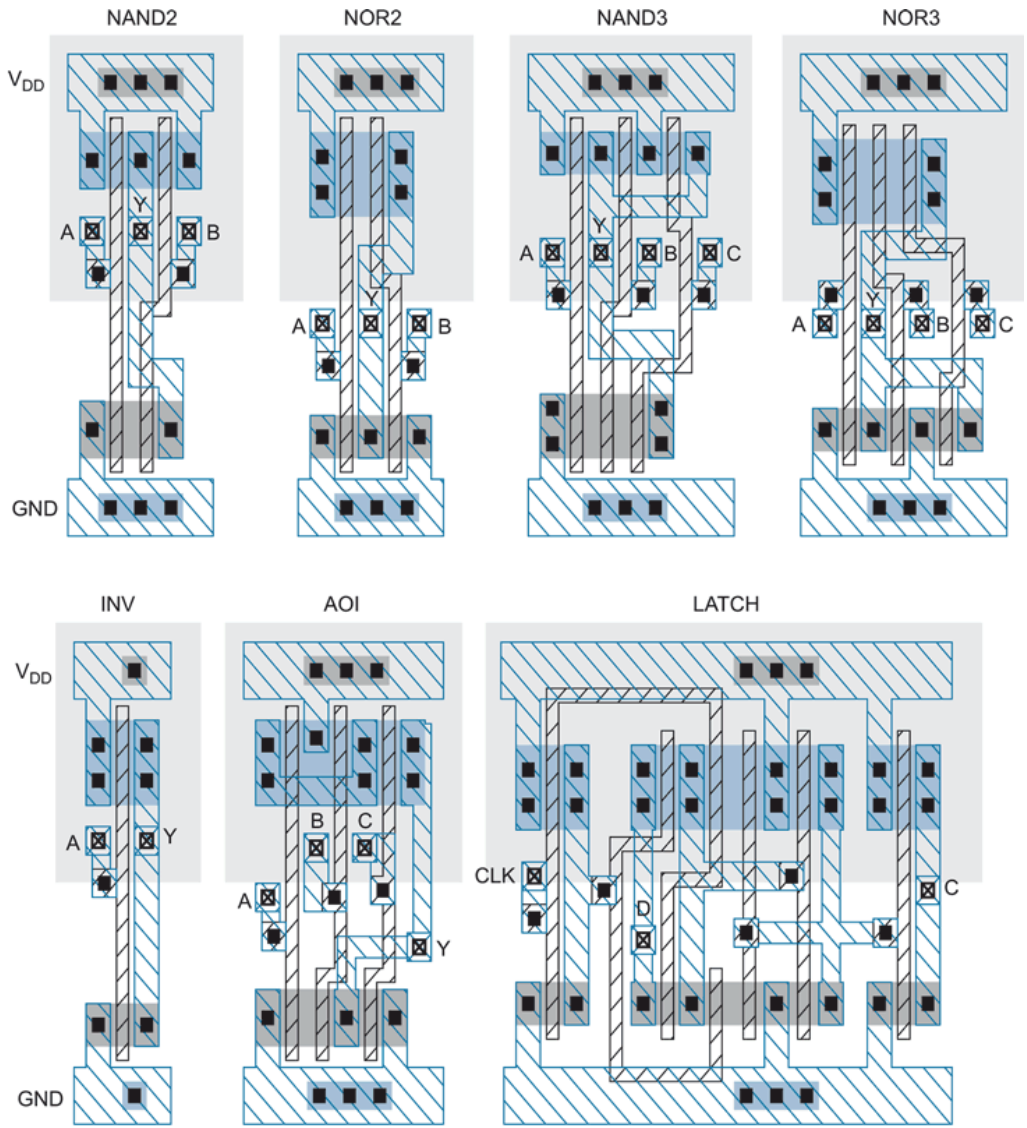


FIG 1.62 Simple standard cell library. Color version on inside front cover.

More Layout Examples

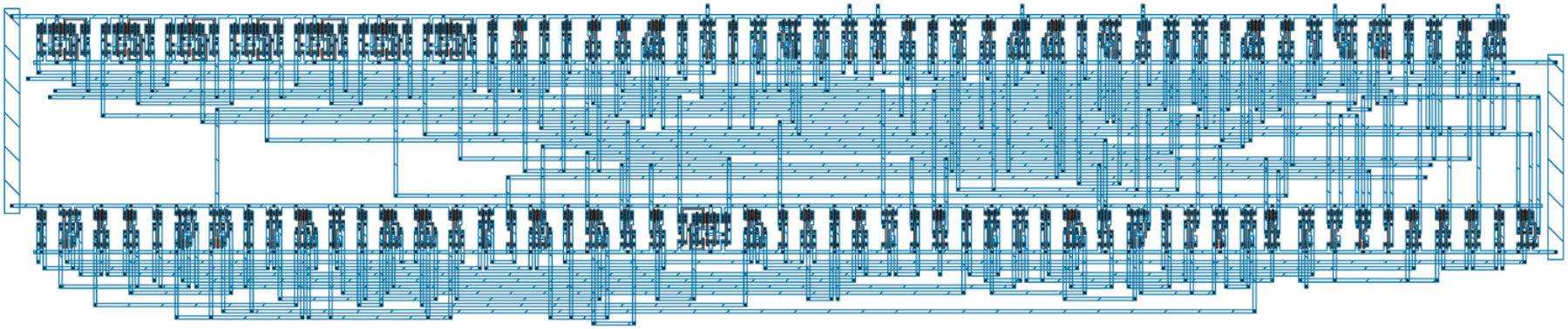


FIG 1.63 MIPS controller layout