Interconnect

Analysis of interconnect is becoming as important as transistors in modern processes.

Modern processes use 6-10 metal layers

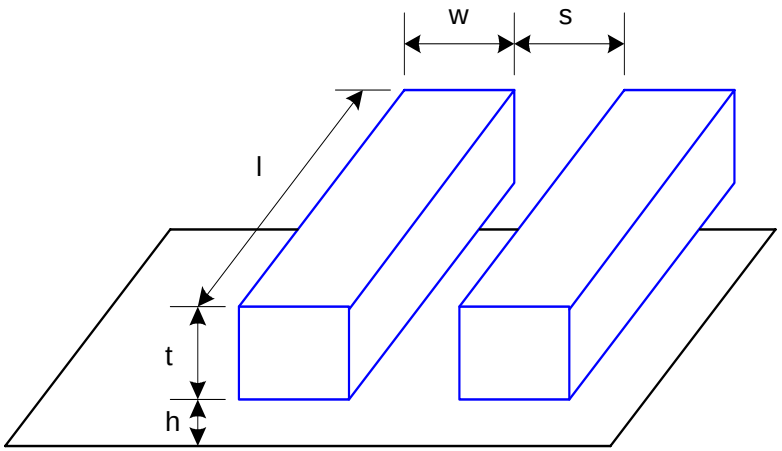
Layer stack for 180nm process

Pitch = w + s

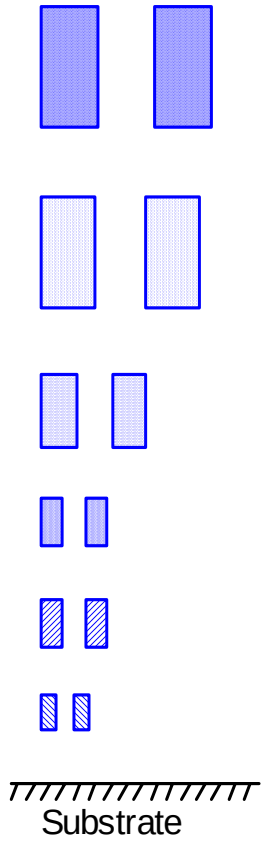
Aspect Ratio = t / w

Newer processes have AR ~ 2

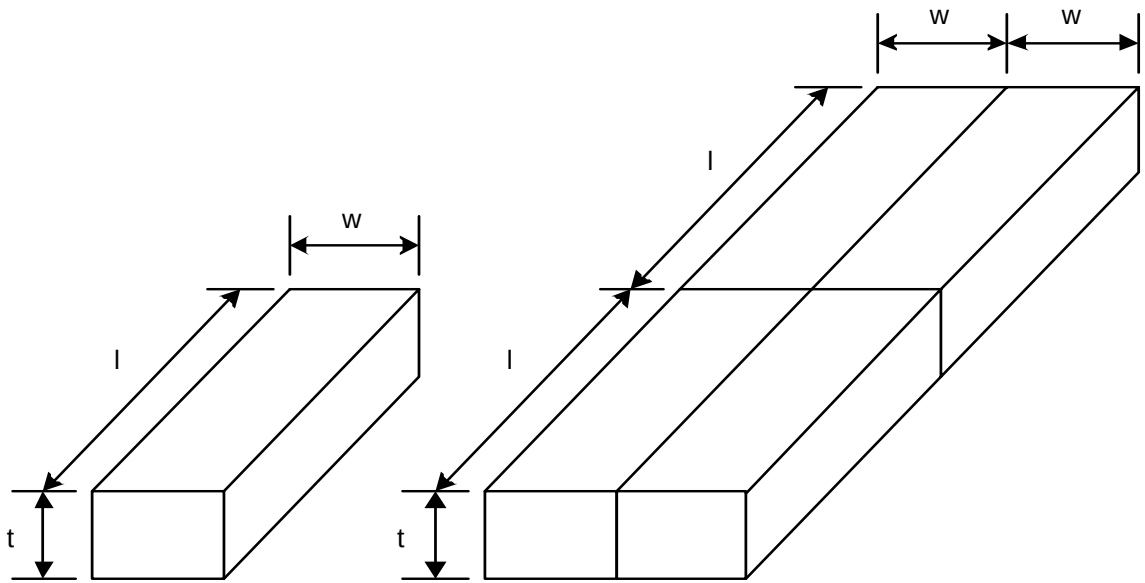
Thicker wires as you move towards upper metal layers



Layer	T (nm)	W (nm)	S (nm)	AR
	1000			
6	1720	860	860	2.0
	1000			
5	1600	800	800	2.0
	1000			
4	1080	540	540	2.0
	700			
3	700	320	320	2.2
	700			
2	700	320	320	2.2
	700			
1	480	250	250	1.9
	800			



Wire Resistance



$$\rho = resistivity (\Omega m)$$

$$R = \frac{\rho}{t}\frac{l}{w} = R_{\square}\frac{l}{w}$$

$$R_{\square} = \textit{sheet resistance} \quad (\Omega/\square)$$

Count number of squares and multiply by sheet resistance to get R

Wire Resistance

Older processes used aluminum, today's processes use copper

Special barrier layer required to stop copper from diffusing into silicon and destroying transistors

Typical sheet resistance values in 180nm process

Layer	Sheet Resistance (Ω/□)
Diffusion (silicided)	3-10
Diffusion (unsilicided)	50-200
Polysilicon (silicided)	3-10
Polysilicon (unsilicided)	50-400
Metal1	0.08
Metal2	0.05
Metal3	0.05
Metal4	0.03
Metal5	0.02
Metal6	0.02

Contact Resistance

Contacts and vias also have about 2-20 Ω of resistance.

Higher resistance than that of metal wires.

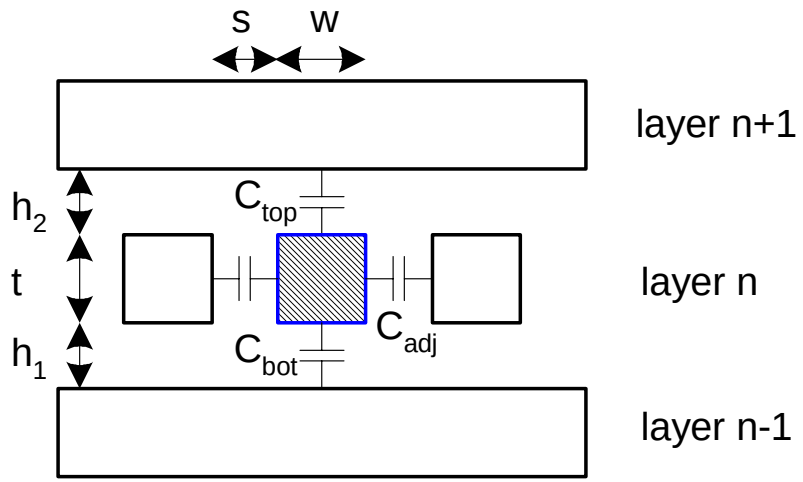
Use many contacts to get lower R

As current crowds at the periphery, many small contacts required rather than one huge contact.

Wire Capacitance

Wire have capacitance per unit length to neighboring layers and layers above and below

$$C_{total} = C_{bottom} + C_{top} + 2C_{adjacent}$$



Parallel plate capacitance equation $C = \varepsilon A / d$

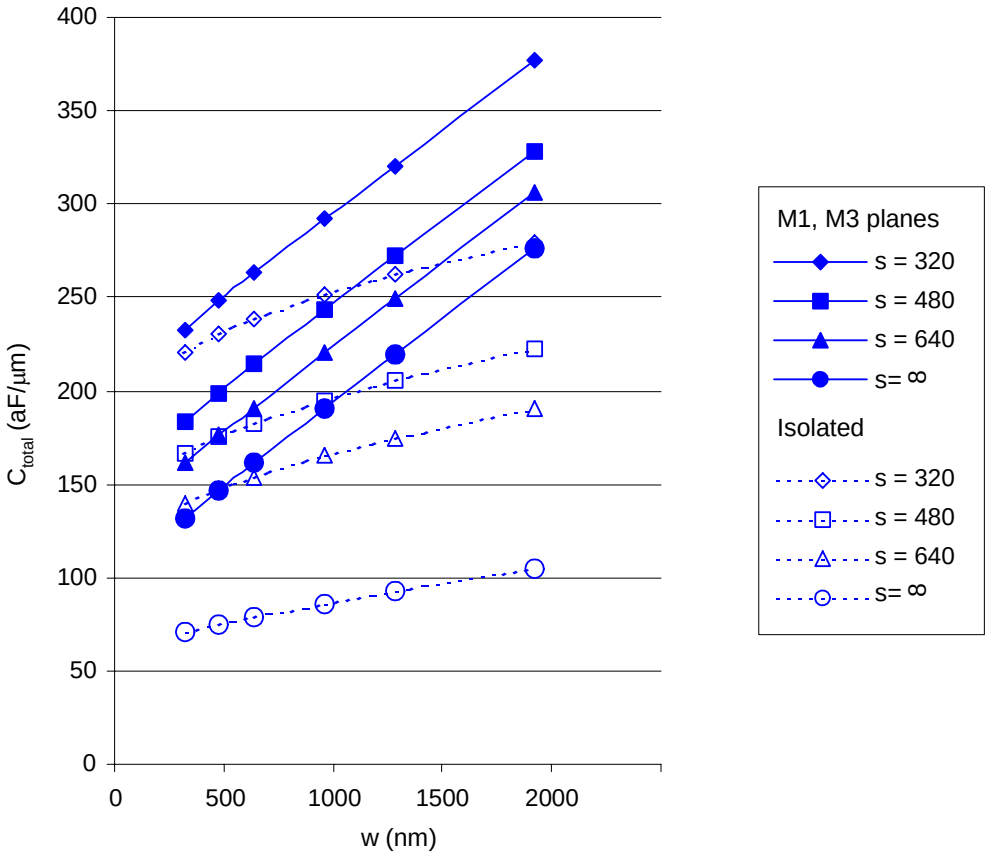
- Wires are not truly parallel plate, but obey trends
- Increasing area (W or t) increases capacitance
- Increasing distance (s or h) decreases capacitance

Wire Capacitance

Dielectric constant in the previous equation $\varepsilon = k\varepsilon_0$

$\varepsilon_0 = 8.85 \times 10^{-14}$F/cm and k = 3.9 for SiO_2

Newer processes are starting to use low-k dielectric materials to reduce capacitance



Typically wire have ~0.2fF/µm

Gate capacitance ~2fF/µm

Diffusion and Polysilicon Capacitance

Diffusion capacitance is very high (~2fF/μm)

- Comparable to gate capacitance
- Diffusion also has high resistance
- Avoid using diffusion runners for wires!!

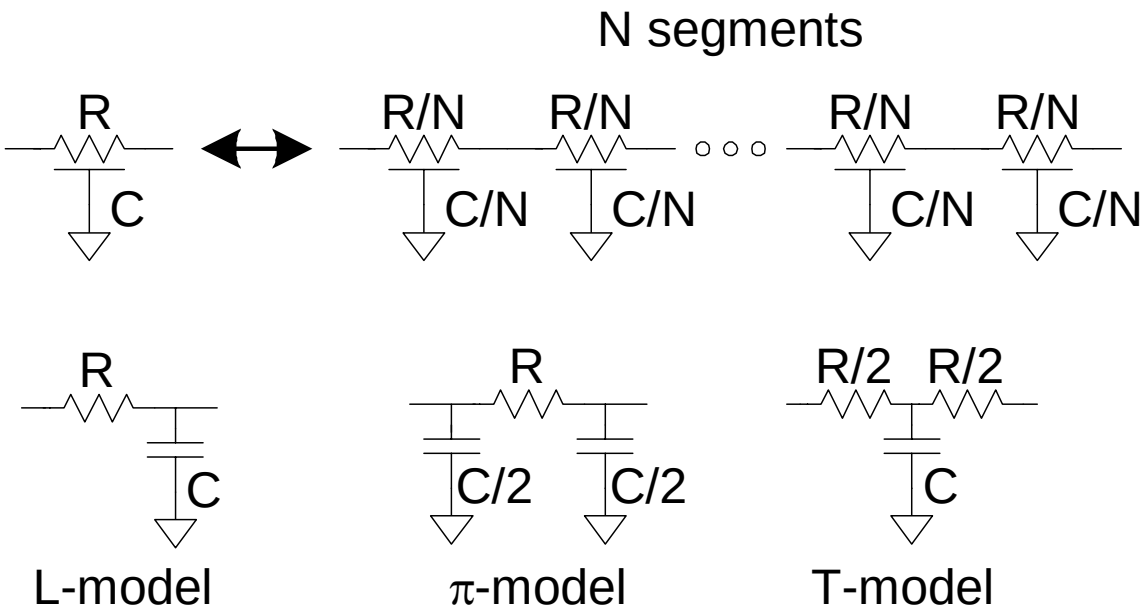
Polysilicon has lower C but higher R

- Use for transistor gates
- Occasionally for very small wires between gates

Wire Delay: Lumped Element Models

Wires are a distributed system

Approximated using lumped element models



3 segment π-model is accurate to within 3% in simulations

L-model would require about 100 segments to obtain the same accuracy

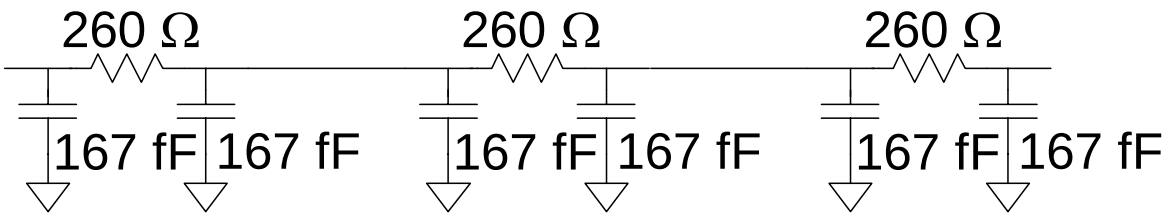
Use single segment π-model for Elmore delay

Wire Delay: Lumped Element Models

Example: Metal2 wire in 180nm process that is 5 mm long and 0.32 μm wide

Construct a 3 segment π-model

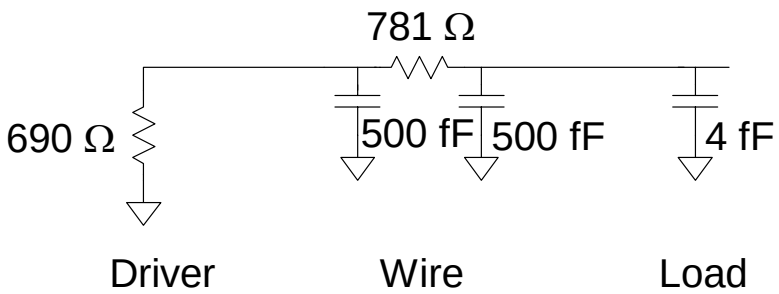
$R_{\square} = 0.05\Omega/\square \Rightarrow R = 781\Omega$ and $C_{permicron} = 0.2fF/\mu m \Rightarrow C = 1pF$



Estimate delay of 10x inverter driving a 2x inverter at the end of the above wire

$R = 2.5k\Omega \times \mu m$ for gates

Unit inverter: 0.36 μm for NMOS, 0.72 μm for PMOS



t_{pd} = 1.1 ns

Crosstalk

A capacitor does not like to change its voltage instantaneously

A wire has high capacitance to its neighbor

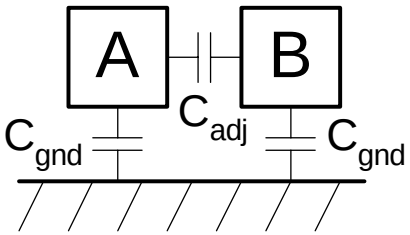
When neighbor switches from 1-> 0 or 0 -> 1 the wire tends to switch too

Called ***capacitive coupling*** or ***crosstalk***

Effects: Noise on non-switching wires and increased delay on switching wires

Assume wires above and below on average are quiet and there-for second terminal of capacitor can be ignored

Modeled as $C_{gnd} = C_{top} + C_{bottom}$



Effective $C_{adjacent}$ depends on behavior of neighbors

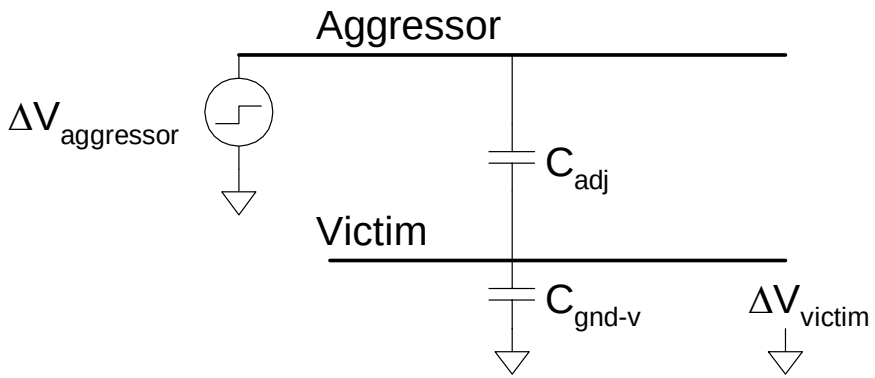
Miller Effect (Miller Coupling Factor MCF)

B	*DV*	$C_{eff(A)}$	*MCF*
constant	V_{DD}	$C_{gnd} + C_{adjacent}$	1
switching same direction as A	0	C_{gnd}	0
switching opposite direction as A	$2V_{DD}$	$C_{gnd} + 2C_{adjacent}$	2

Crosstalk

Crosstalk causes noise on non-switching wires

If the victim is floating
model as capacitive voltage divider

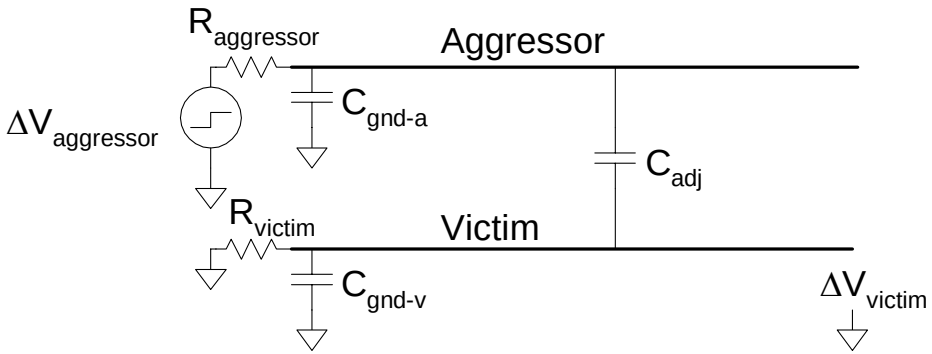


$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \Delta V_{aggressor}$$

Crosstalk Noise: Victim

Usually victim is driven by a gate that fights noise

- Noise depends on relative resistances
- Victim driver is in linear region, aggressor in saturation
- If sizes are same, $R_{aggresor}$ = 2-4 x R_{victim}

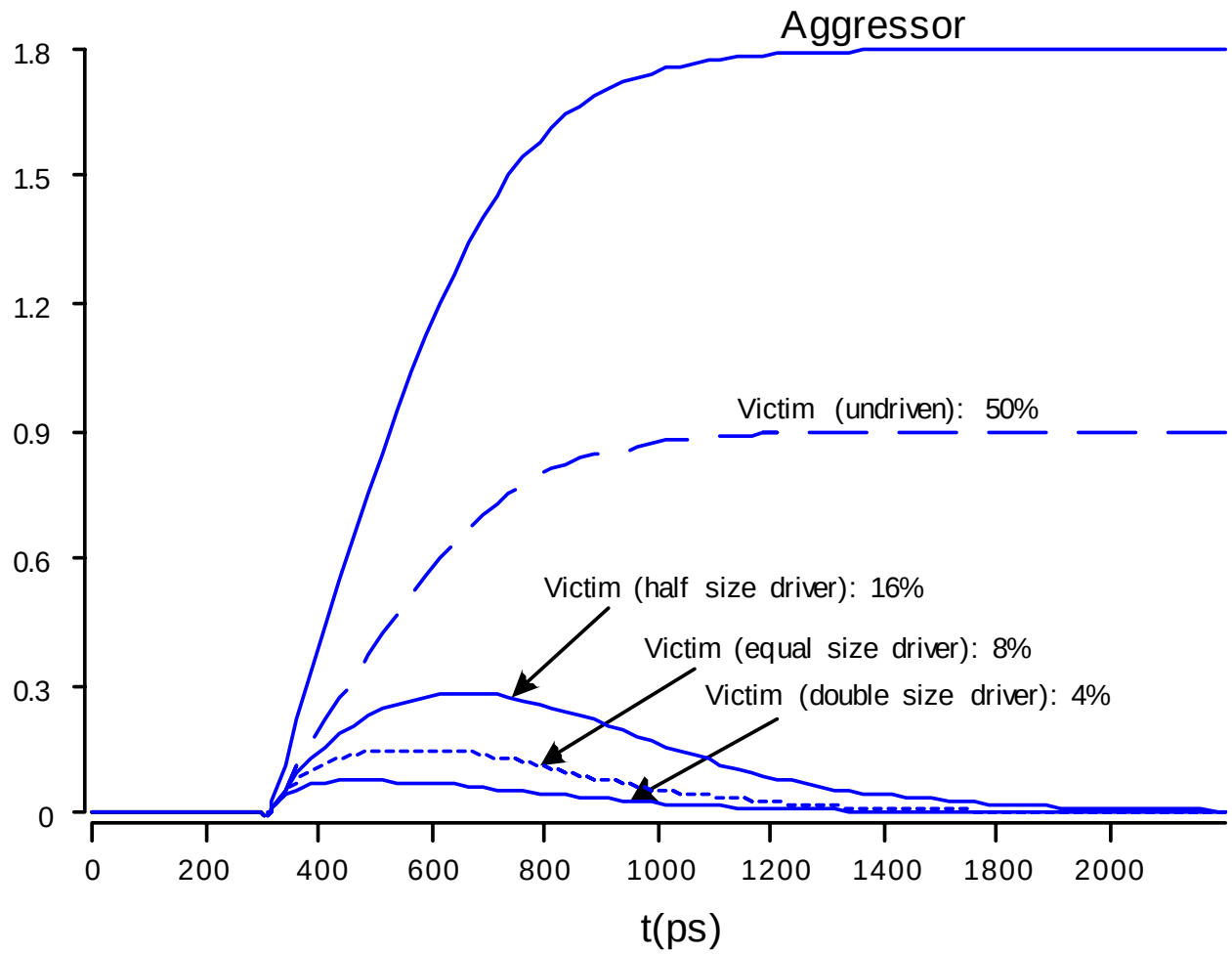


$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \frac{1}{1+k} \Delta V_{aggressor}$$

$$k = \frac{\tau_{aggressor}}{\tau_{victim}} = \frac{R_{aggressor}(C_{gnd-a} + C_{adj})}{R_{victim}(C_{gnd-v} + C_{adj})}$$

Crosstalk Coupling: Waveforms

Simulated coupling for $C_{adj} = C_{victim}$



Crosstalk noise

Noise implications:

If the noise is less than the noise margin nothing happens

Static CMOS logic will eventually settle to correct output even if disturbed by a large noise spike

- But these glitches cause extra delay
- Also causes extra power from false transitions

Dynamic logic (discussed later) will never recover from noise

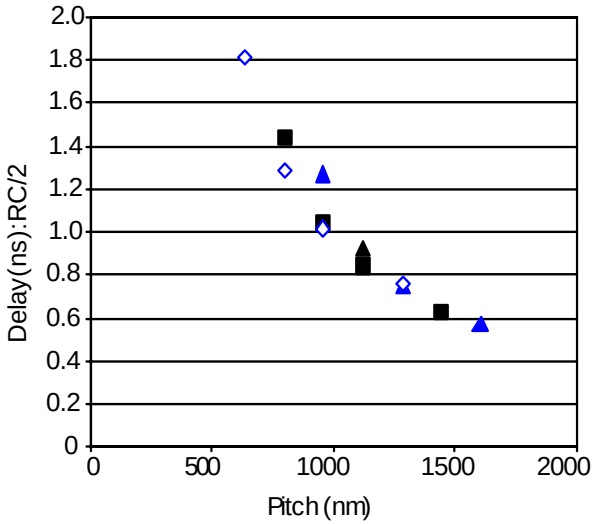
Memories and other sensitive circuits can also produce wrong answers

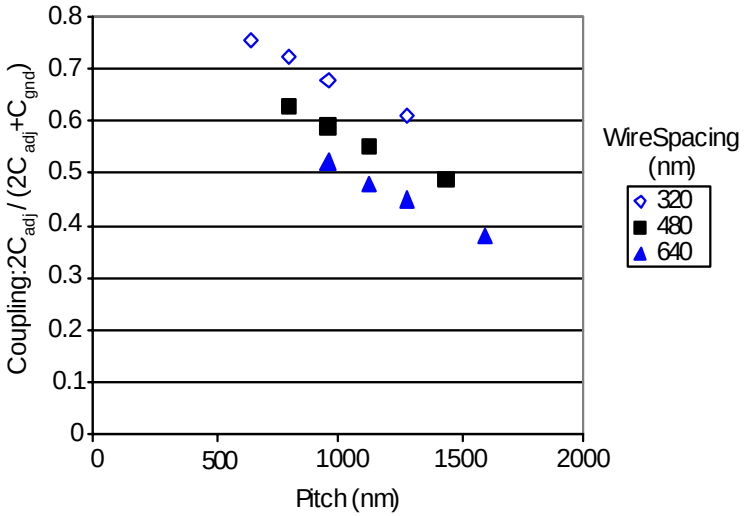
Wire Engineering

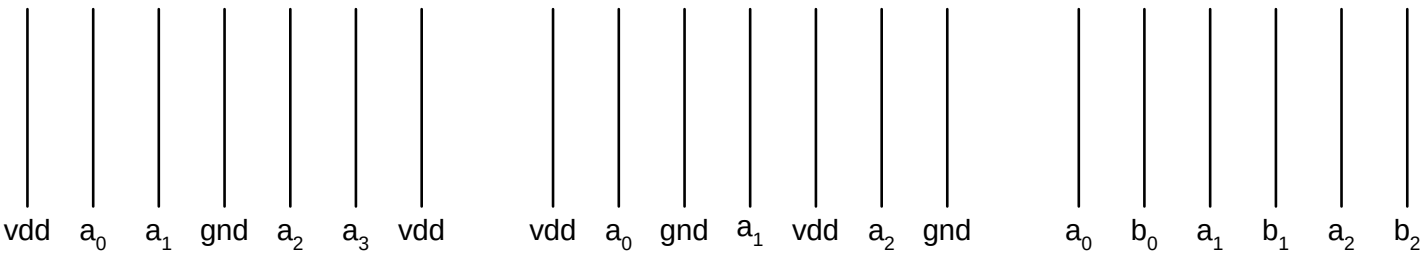
Goal: Achieve delay, area and power specifications with acceptable noise

Degrees of freedom

- Width, Spacing, Layer and Shielding







Repeaters

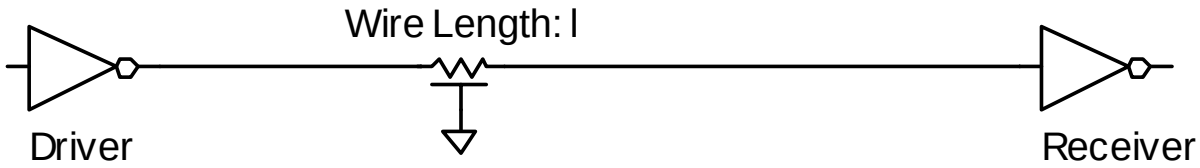
R and C are proportional to l

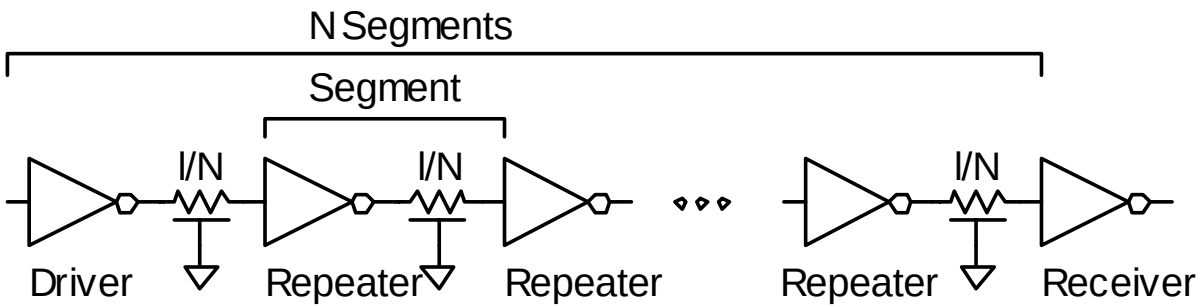
RC delay is proportional to l^2

Unacceptably high for long wires

Break long wires into N shorter segments

Drive each segment with an inverter or buffer





Repeaters

How many repeaters should we use?

How large should each one be?

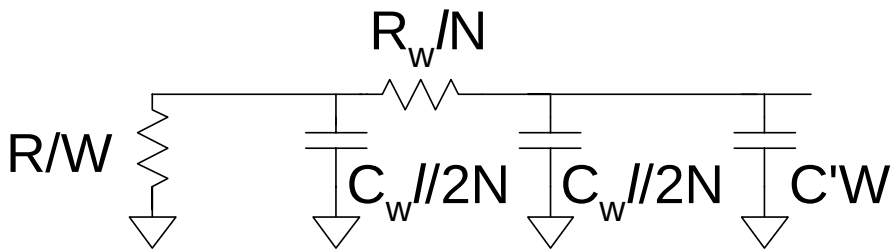
Equivalent circuit

- Wire length ***l***

  Wire capacitance $C_w * l$, Resistance $R_w * l$

- Inverter width W (NMOS = W, PMOS = 2W)

  Gate capacitance **C`* W**, Resistance **R / W**



Repeaters

Write equation for Elmore Delay

Differentiate with respect to W and N

Set equal to 0 and solve

Best length of wire between repeaters, neglecting diffusion parasitics

$$\frac{l}{N} = \sqrt{\frac{2RC'}{R_w C_w}}$$

Delay per unit length of a properly repeated wire is

$$\frac{t_{pd}}{l} = (2 + \sqrt{2})\sqrt{RC' R_w C_w}$$

NMOS transistor width to achieve this delay

$$W = \sqrt{\frac{RC_w}{R_w C'}}$$