## Power Dissipation

Static CMOS gates in older technologies were very power-efficient.

In newer technologies, power is a primary design constraint.

Power dissipation has skyrocketed due to transistor scaling, chip transistor counts and clock frequencies.

### Instantaneous Power

The instantaneous power P(t) drawn from the power supply is proportional to the supply current $i_{DD}(t)$ and the supply voltage $V_{DD}$.

$$P(t) = i_{DD}(t)V_{DD}$$

### Energy

The energy consumed over the time interval T is the integral of P(t)

$$E = \int_0^T i_{DD}(t)V_{DD}dt$$

### Average Power

The average power over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$$

## *CMOS Power Dissipation*

Power dissipation in CMOS circuits comes from two components

- Static dissipation due to
  - subthreshold conduction through OFF transistors
  - tunneling current through gate oxide
  - leakage through reverse-biased diodes
  - contention current in ratioed circuits
- Dynamic dissipation due to
  - charging and discharging of load capacitances
  - *short circuit* current while both PMOS and NMOS networks are partially ON

$$P_{total} = P_{static} + P_{dynamic}$$

We have discussed most of the static dissipation factors before.

Below 130nm static power is rapidly becoming a primary design issue

Eventually, static power dissipation may become comparable to dynamic power

Ratioed circuits (e.g. pseudo NMOS, discussed later) have more static dissipation.

## Dynamic Power Dissipation

Primary source of dynamic dissipation is charging of the load capacitance.

Suppose load **C** is switched between $V_{DD}$ and GND at average frequency $\mathbf{f_{sw}}$.

Over time **T**, load is charged and discharged $\mathbf{Tf_{sw}}$ times.

In one complete charge/discharge cycle, a total charge of $\mathbf{Q=CV_{DD}}$ is transferred between $V_{DD}$ and GND

The average dynamic power dissipation is

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt = \frac{V_{DD}}{T}\int_0^T i_{DD}(t)dt$$

Taking the integral of the current over interval T as the total charge delivered during time T

$$P_{dynamic} = \frac{V_{DD}}{T}[Tf_{sw}CV_{DD}] = CV_{DD}^2 f_{sw}$$

As not all gates switch every clock cycle the above quantity is multiplied by $\alpha$.

$\alpha$=1 for clock, for data maximum is $\alpha$=0.5, empirically static CMOS has $\alpha$=0.1

Also due to non-zero input rise and fall times (slew), both NMOS and PMOS will be ON.

Causes short circuit current that depends on input slew and output capacitance.