Capacitance

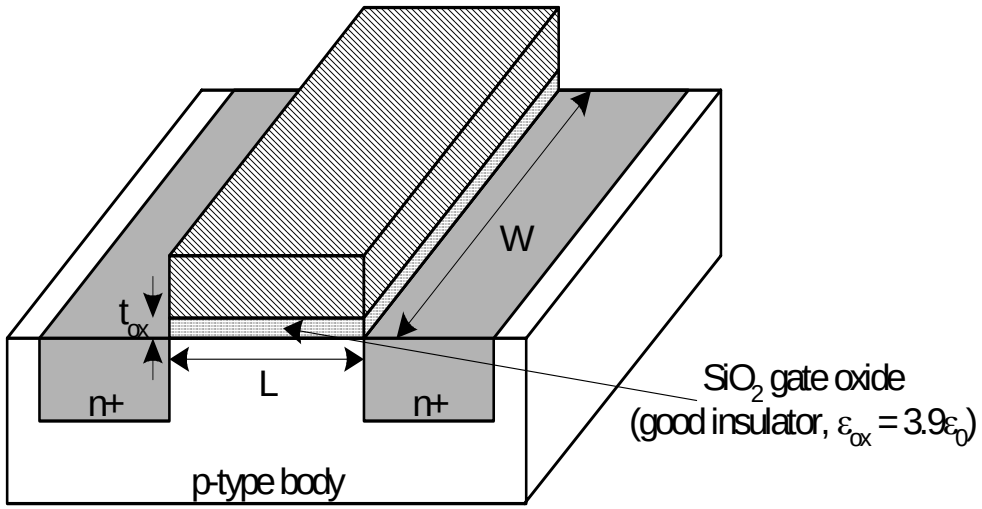
Any two conductors separated by an insulator form a parallel-plate capacitor.

Gate capacitance is very important as it creates channel charge necessary for operation.

Source and Drain have capacitance to body

- Across reverse-biased diodes
- Called ***diffusion capacitance*** because it is associated with source/drain diffusion.

Gate capacitance



Approximate channel as connected to source

.

$$C_{gs} = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL$$
$$= C_{permicron} W$$

$C_{permicron}$ is typically 2fF/μm.

Diffusion Capacitance

C_{sb}, C_{db}

Undesirable, called parasitic capacitance.

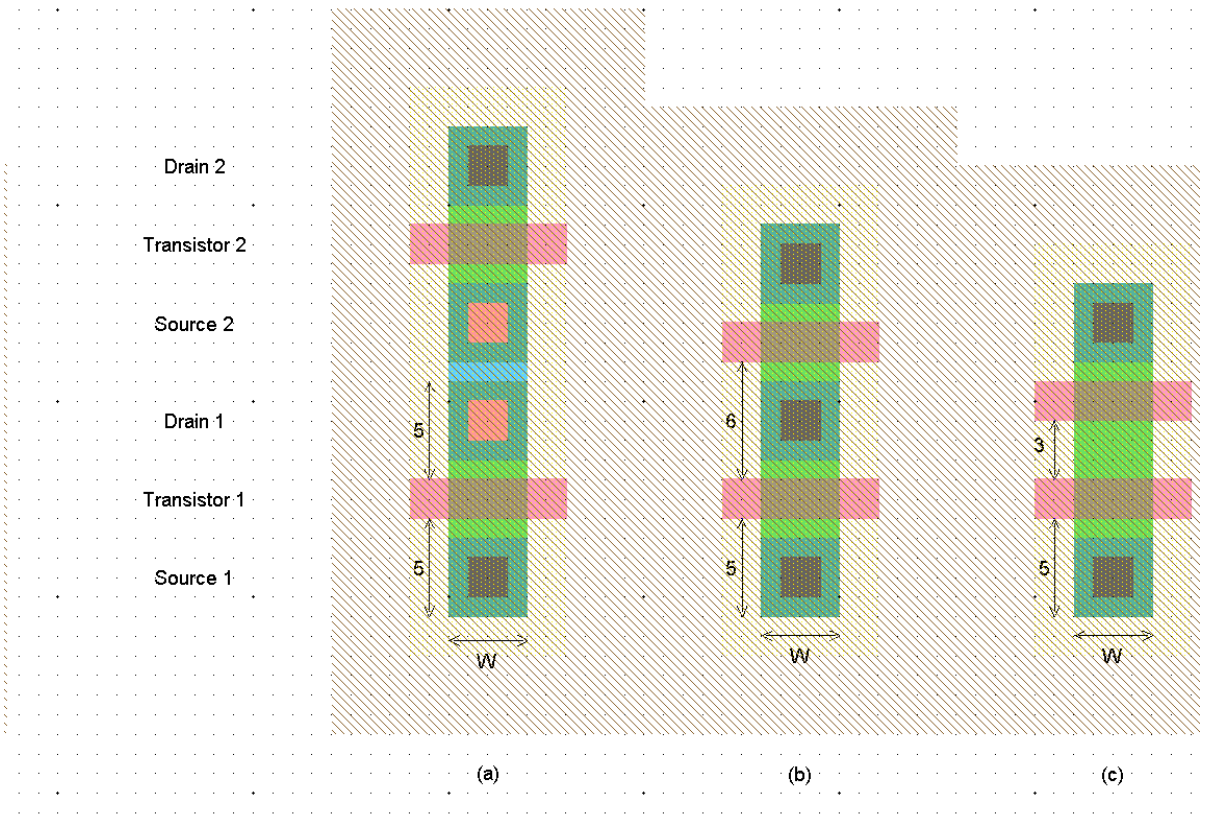
Capacitance depends on area and perimeter

Use small diffusion nodes

Comparable to C_g for contacted diffusion

Half of C_g for uncontacted diffusion.

Varies with process

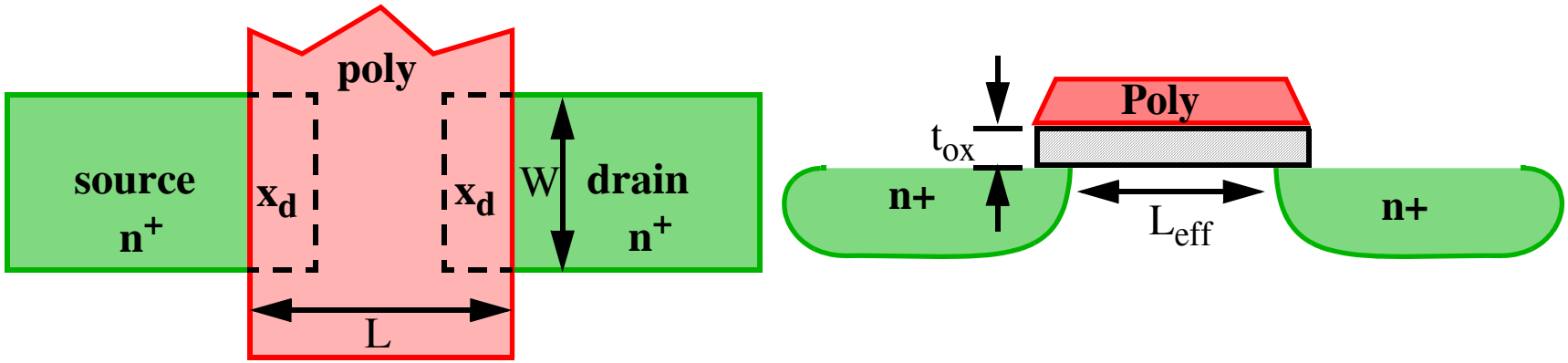


Gate Capacitance Details

The gate capacitance can be decomposed into several parts:

- One part contributes to the channel charge.
- A second part is due to the topological structure of the transistor.

MOS Structure Capacitances, Overlap:



Lateral diffusion: source and drain diffusion extend under the oxide by an amount x_d.

The effective channel length (L_{eff}) is less than the *drawn length* L by $2*x_d$.

This gives rise to a linear, fixed capacitance called *overlap capacitance*.

$$C_{gsO} = C_{gdO} = C_{ox}x_d W = C_O W$$

Since x_d is technology dependent, it is usually combined with C_{ox}.

Gate Capacitance Details

Channel Charge

The gate-to-channel capacitance is composed of three components, C_{gs}, C_{gd} and C_{gb}.

Each of these is non-linear and dependent on the region of operation.

Estimates or average values are often used

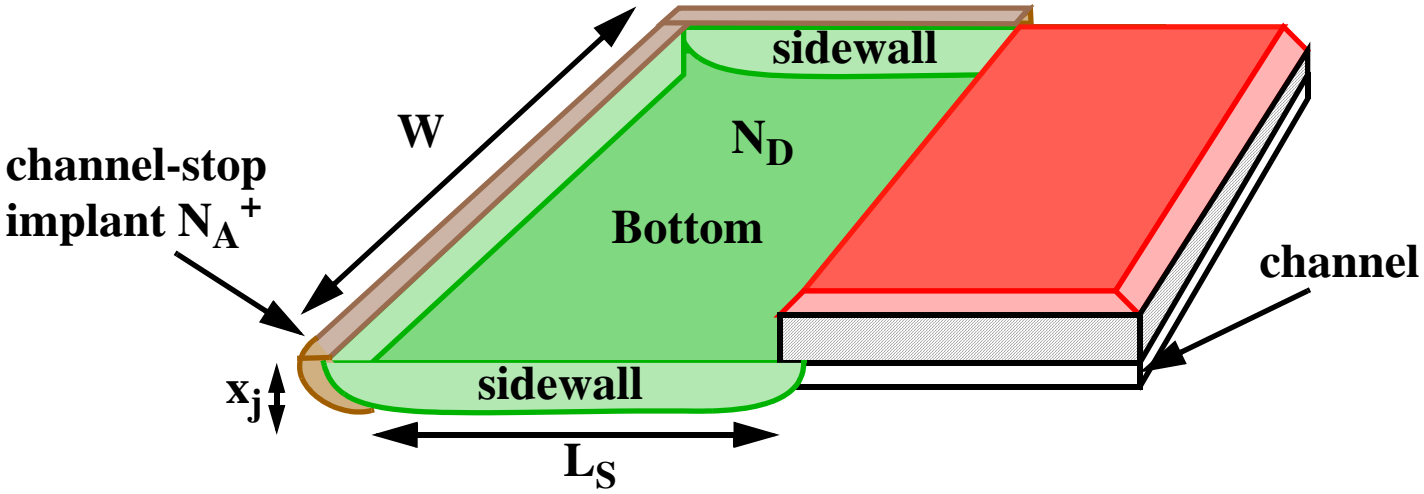
- Linear: C_{gb} ~=0 since the inversion region shields the bulk electrode from the gate.
- Saturation: C_{gb} and C_{gd} is ~= 0 since the channel is pinched off.

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Linear	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Diffusion Capacitance Details

Junction or Diffusion Capacitances

This component is caused by the reverse-biased source-bulk and drain-bulk *pn-junctions*. This capacitance is ***non-linear*** and *decreases* as reverse-bias is *increased*.



Bottom-plate junction

Depletion region capacitance is

$$C_{bottom} = C_j W L_S$$

Diffusion Capacitance Details

C_j is the junction capacitance per unit area.

$$C_j = C_{j0}\left(1 + \frac{V_{sb}}{\Psi_0}\right)^{-M_j}$$

where, C_{j0} is the junction capacitance at zero bias and is highly process dependent.

M_j is the junction grading coefficient, typically between 0.5 and 0.33 depending on the abruptness of the diffusion junction.

Ψ_0 is the built-in potential that depends on doping levels given by

$$\Psi_0 = \upsilon_T \ln\left(\frac{N_A N_D}{N_i^2}\right)$$

where, υ_T is the thermal voltage.

N_A and N_D are doping levels of the body and source diffusion region.

N_i is the intrinsic carrier concentration in undoped silicon.

Diffusion Capacitance Details

Side-Wall Capacitance

Formed by the source region with doping N_D and the p^+channel-stop implant with doping N_A^+.

Since the channel-stop doping is usually higher than the substrate, this results in a higher unit capacitance:

$$C_{sw} = C'_{jsw} x_j (W + 2 \times L_S)$$

C'_{jsw} is similar to C_j but with different coefficients.M_j = 0.33 to 0.5.

Note that the channel side is not included in the calculation. Some SPICE models have an extra parameter to account for this junction.

x_j is usually technology dependent and combined with C'_{jsw} as C_{jsw}.

Total diffusion/junction capacitance is:

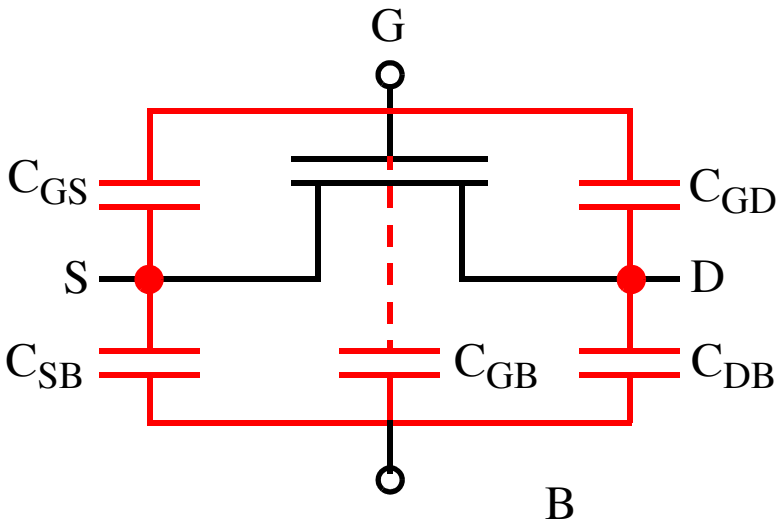
$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$

$$C_{diff} = C_j L_S W + C_{jsw}(2L_S + W)$$

MOS Capacitance Model

Capacitive Device Model

The previous model can be summarized as:



$C_{GS} = C_{gs} + C_{gsO}$

$C_{GD} = C_{gd} + C_{gdO}$

$C_{GB} = C_{gb}$

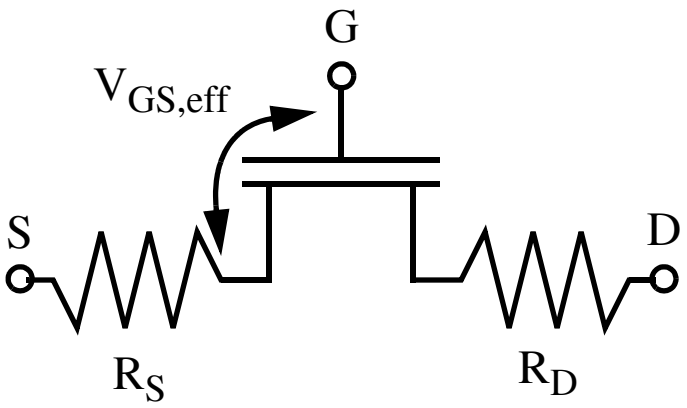
$C_{SB} = C_{Sdiff}$

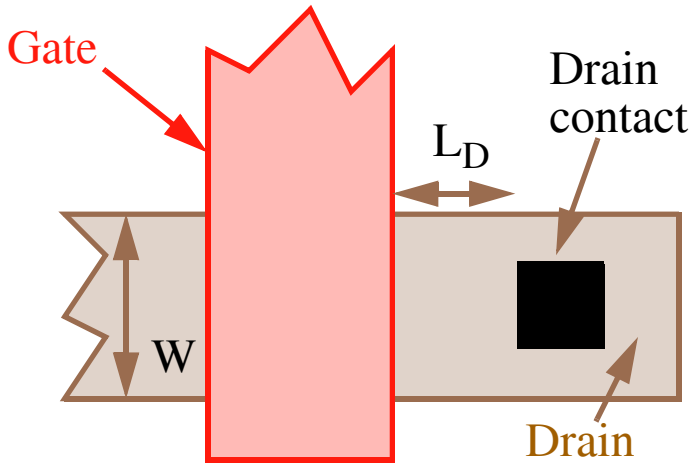
$C_{DB} = C_{Ddiff}$

The dynamic performance of digital circuits is directly proportional to these capacitances!

Source-Drain Resistance

Scaling causes junctions to be *shallower* and contact openings to be *smaller*.
This increases the parasitic resistance in series with the source and drain regions:





This resistance can be expressed as:

$$R_{S,D} = \frac{L_{S,D}}{W} R_{\square} + R_C$$

R_C = Contact Resistance
$R_{\square}$ = Sheet resistance ($50\Omega - 1k\Omega$)
$L_{S,D}$ = length of source/drain region.

The series resistance degrades device performance by decreasing drain current.
One option is to cover drain and source regions with a low-resistivity material such as *titanium* or *tungsten*.

This process is called ***silicidation***, and is used in reducing poly resistance as well.

Capacitance Example

Given:

$t_{ox} = 20nm$ $\quad x_d = 0.15um$

$L = 1.2um$ $\quad C_{j0} = 3 \times 10^{-4} F/m^2$

$W = 1.8um$

$L_D = L_S = 3.6um$ $\quad C_{jsw0} = 8 \times 10^{-10} F/m$

Determine the zero-bias value of all relevant capacitances.

Gate capacitance, C_{ox}, per unit area is derived as:

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.5 \times 10^{-2} fF/um}{20 \times 10^{-3} um} = 1.75 fF/um^2$$

Total gate capacitance C_g is:

$$C_g = WLC_{ox} = 1.8um \times 1.2um \times 1.75 fF/um^2 = 3.78 fF$$

Overlap capacitance is:

$$C_{GSO} = C_{GDO} = Wx_dC_{ox} = 0.47 fF$$

Subtracting out overlap capacitance yields C_{gb} under zero-bias:

$$C_{gb} = C_{ox}WL_{eff} = 3.78 - 2 \times 0.47 = 2.84 fF$$

Capacitance Example

Diffusion capacitance is the sum of bottom:

$$C_{j0}L_D W = 3\times10^{-1} fF/um^2 \times 3.6um \times 1.8um = 1.95fF$$

Plus side-wall (under zero-bias):

$$C_{jsw0}(2L_D + W) = 8\times10^{-1}(2 \times 3.6um + 1.8um) = 7.2fF$$

In this example, diffusion capacitance dominates gate capacitance (3.78fF versus 9.2fF).

Note that this is the worst case condition. Increasing reverse bias reduces diffusion capacitance (by about 50%).

Also note that side-wall dominates diffusion. Advanced processes use SiO_2 to isolate devices (trench isolation) instead of N_A^+ implant.