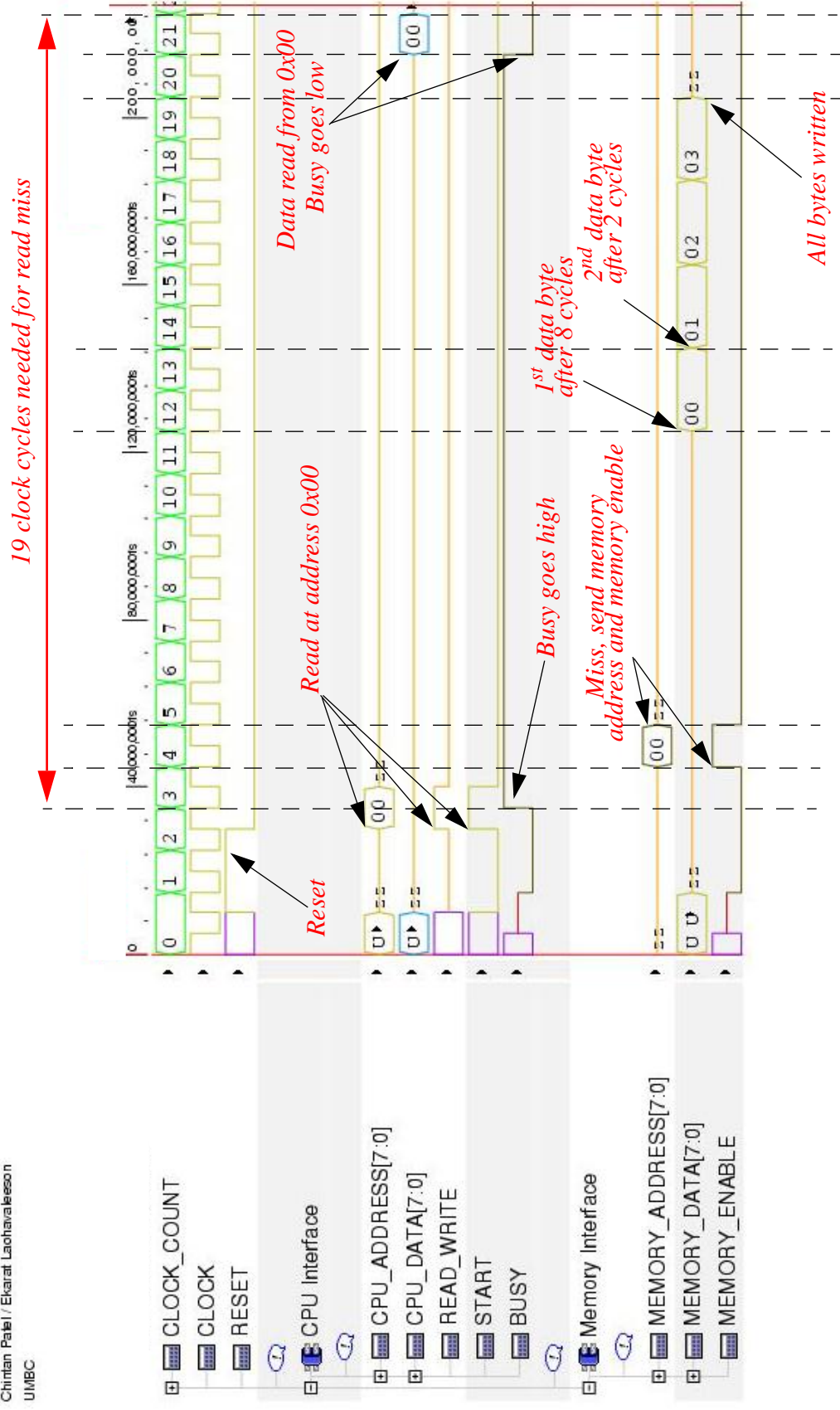


Two cycles of Reset = 1, followed by a read request at address 00000000, that causes a read miss

Project Waveforms: READ MISS

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*Write to 0x03, block already in cache due to the read miss, write data 0xFF
 Read from 0x03, data written above
 Write to 0xFF, block not in cache, causes a miss, write data 0xAA, no change in cache data, no need to access memory*

Project Waveforms: WRITE HIT/ READ HIT/ WRITE MISS

