LAB Assignment #3 for CMPE 315

Assigned: Thrs, Sep 23rd
Due: Mon, Oct 4th

Description: Create a compact layout and perform simulations for the following gates

- Draw the layout for a minimum sized inverter and size transistors according to the INVx1 schematic from lab2. Use the simulation and config views from the previous lab to run simulations to verify your layout. Perform simulations with four INVx1 cells connected as load from the previous lab.
- Draw the layout for the NAND2x1 and NOR2x1 cells from the previous lab again using same transistor sizes as lab2. Run simulation with four INVx1 as load using the simulation and config views to verify their functionality.
- Draw the schematic and layout for a 4 input OAI and 4 input AOI gates using instances of INVx1, NAND2x1 and NOR2x1. Create schematic view and config views for simulation. Run simulations to verify the functionality of the cells for both the schematic and layout views. Use four INVx1 cells as the load for this simulations.
- All simulations should use 100ps as their input rise and fall times, all load inverters should be simulated with schematic views and the circuits being designed in this lab should be simulated with their extracted views. For the OAI and AOI simulations should be performed with extracted as well as schematic views.

Report Requirements:

1. Write a brief, about 1 page summary on how to draw layouts.
2. Plot the layouts for all the cells that you have designed.
3. Plot simulation results for each of the cells, to show that they are functionally correct.
4. Plot the schematic and the simulation schematic views for the OAI and AOI gates.
5. Create a table that compares the rise and fall times as well as the rising and falling delay obtained from simulations of the cells using their schematic and layout views.
6. Follow the report writing guidelines about captioning figures, plotting results etc. from lab 2.
7. Submit a single pdf file for your report using submit, the class name is cmpe315_cpatel2 and the project name is lab3.

THE LABS ARE INDIVIDUAL EFFORTS: INSTANCES OF CHEATING WILL RESULT IN YOU FAILING THE COURSE.