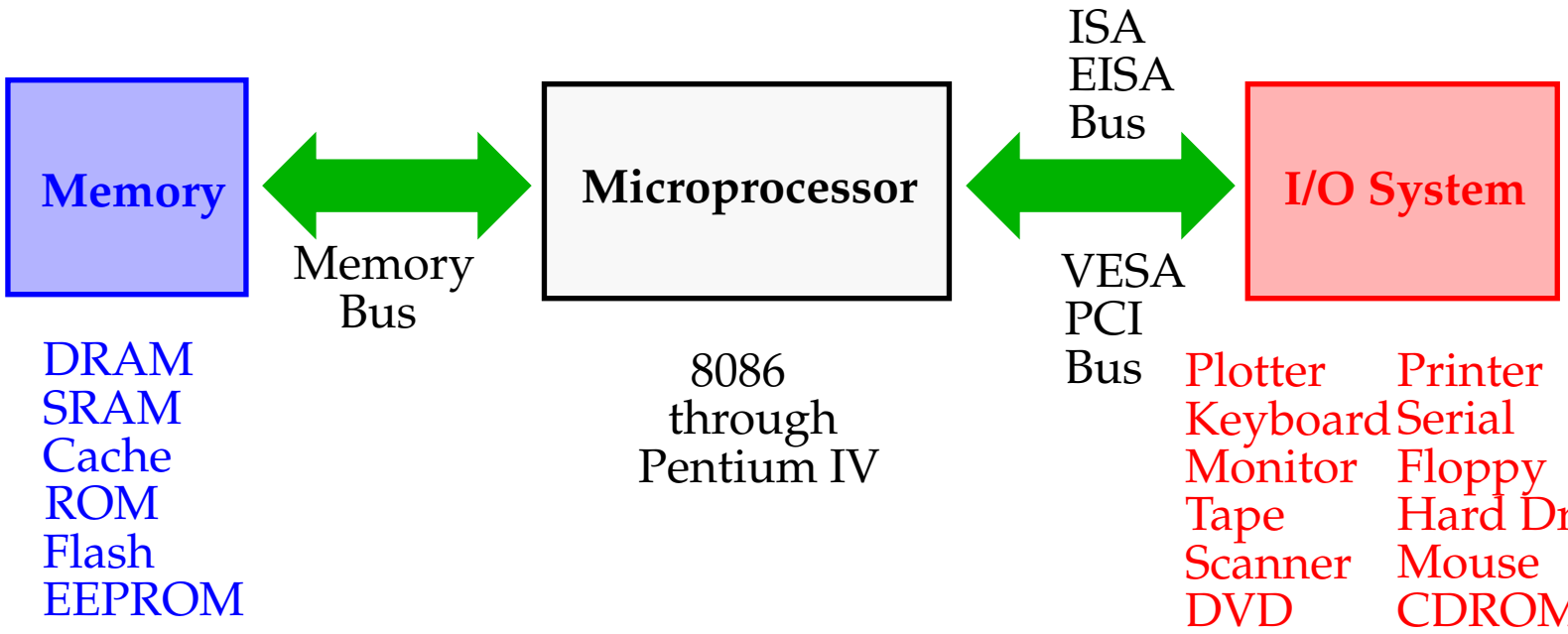
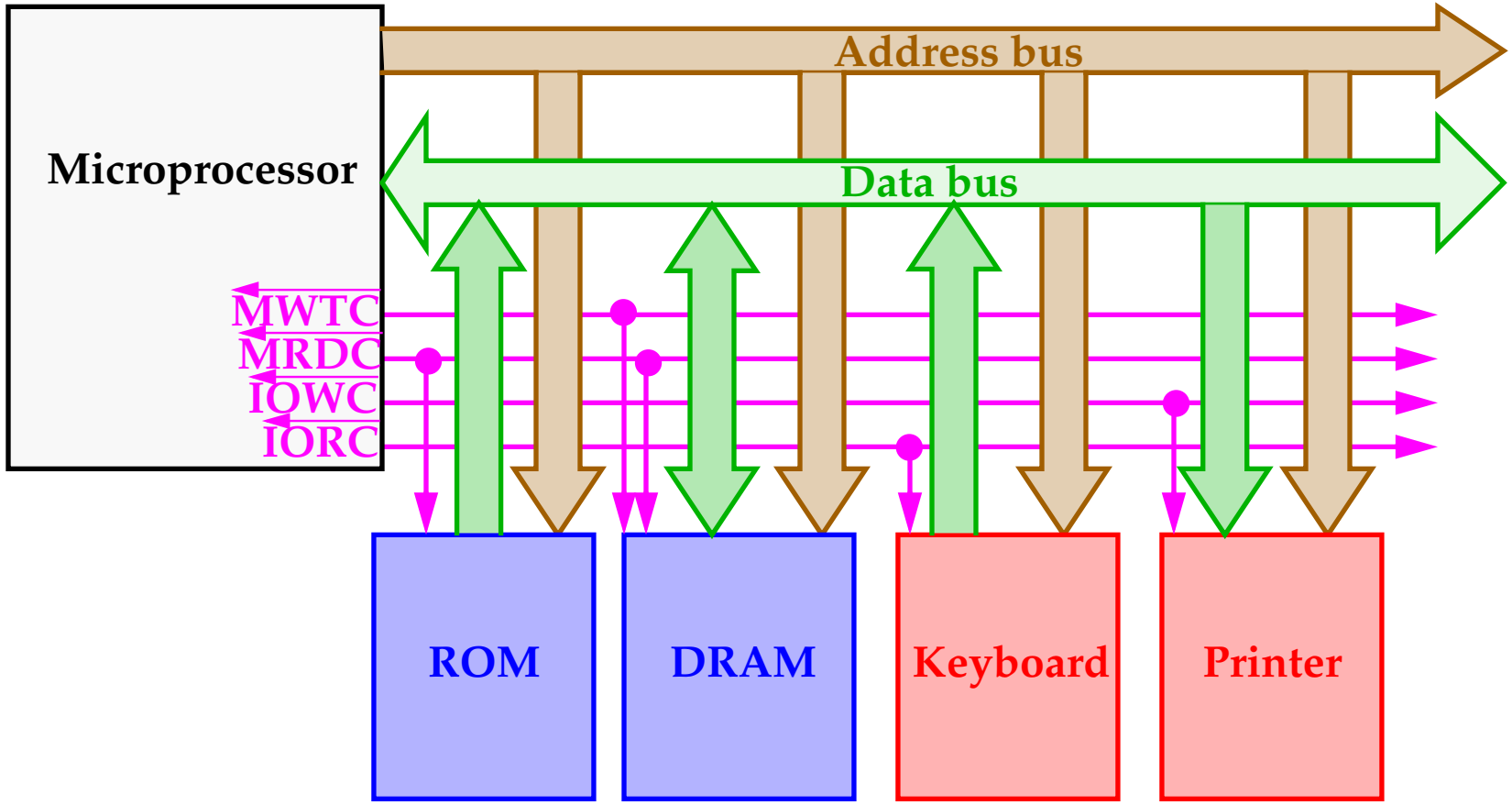
Basic Architecture

Basic components



Basic Architecture

Bus Architecture:



The Pentium bus architecture is not this simple.

We will elaborate on this later.

Basic Bus Architecture

Bus Architecture: Three buses:

- *Address:*

  If I/O, a value between 0000H and FFFFH is issued.

  If memory, it depends on the architecture:

  20-bits (8086/8088)

  24-bits (80286/80386SX)

  25-bits (80386SL/SLC/EX)

  32-bits (80386DX/80486/Pentium)

  36-bits (Pentium Pro/II/III)

- *Data:*

  8-bits (8088)

  16-bits (8086/80286/80386SX/SL/SLC/EX)

  32-bits (80386DX/80486/Pentium)

  64-bits (Pentium/Pro/II/III)

- *Control:*

  Most systems have at least 4 control bus connections (active low).

  $\overline{\textbf{MRDC}}$ (Memory ReaD Control), $\overline{\textbf{MWRC}}$, $\overline{\textbf{IORC}}$ (I/O Read Control), $\overline{\textbf{IOWC}}$.

Basic Bus Architecture

Bus Standards:

- **ISA** (Industry Standard Architecture): 8 MHz
  8-bit (8086/8088)
  16-bit (80286-Pentium)

- **EISA**: 8 MHz
  32-bit (older 386 and 486 machines).

- **PCI** (Peripheral Component Interconnect): 33 MHz
  32-bit or 64-bit (Pentiums)
  New: PCI Express and PCI-X 533 MTS

- **VESA** (Video Electronic Standards Association): Runs at processor speed.
  32-bit or 64-bit (Pentiums)
  Only disk and video. Competes with the PCI but is not popular.

Basic Bus Architecture

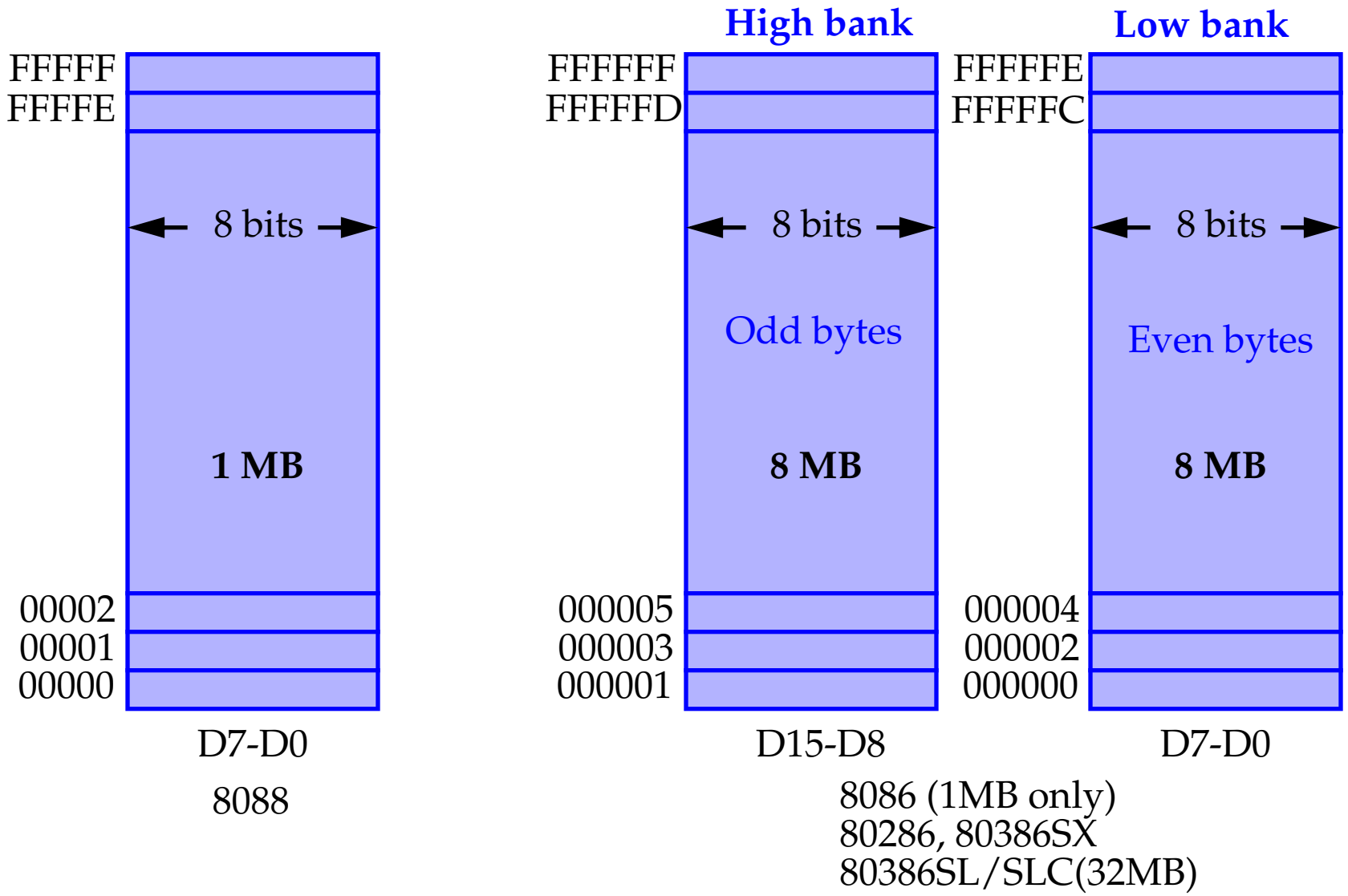
Bus Standards:

- **USB** (Universal Serial Bus): 1.5 Mbps,12 Mbps and now 480 Mbps.
  Newest systems.
  Serial connection to microprocessor.
  For keyboards, the mouse, modems and sound cards.
  - To reduce system cost through fewer wires.

- **AGP** (Advanced Graphics Port): 66MHz
  Newest systems.
  Fast parallel connection: Across 64-bits for 533MB/sec.
  For video cards.
  - To accommodate the new **DVD** (Digital Versatile Disk) players.
  - Latest AGP 3.0 with peak bandwidth of 2.1GB/s.

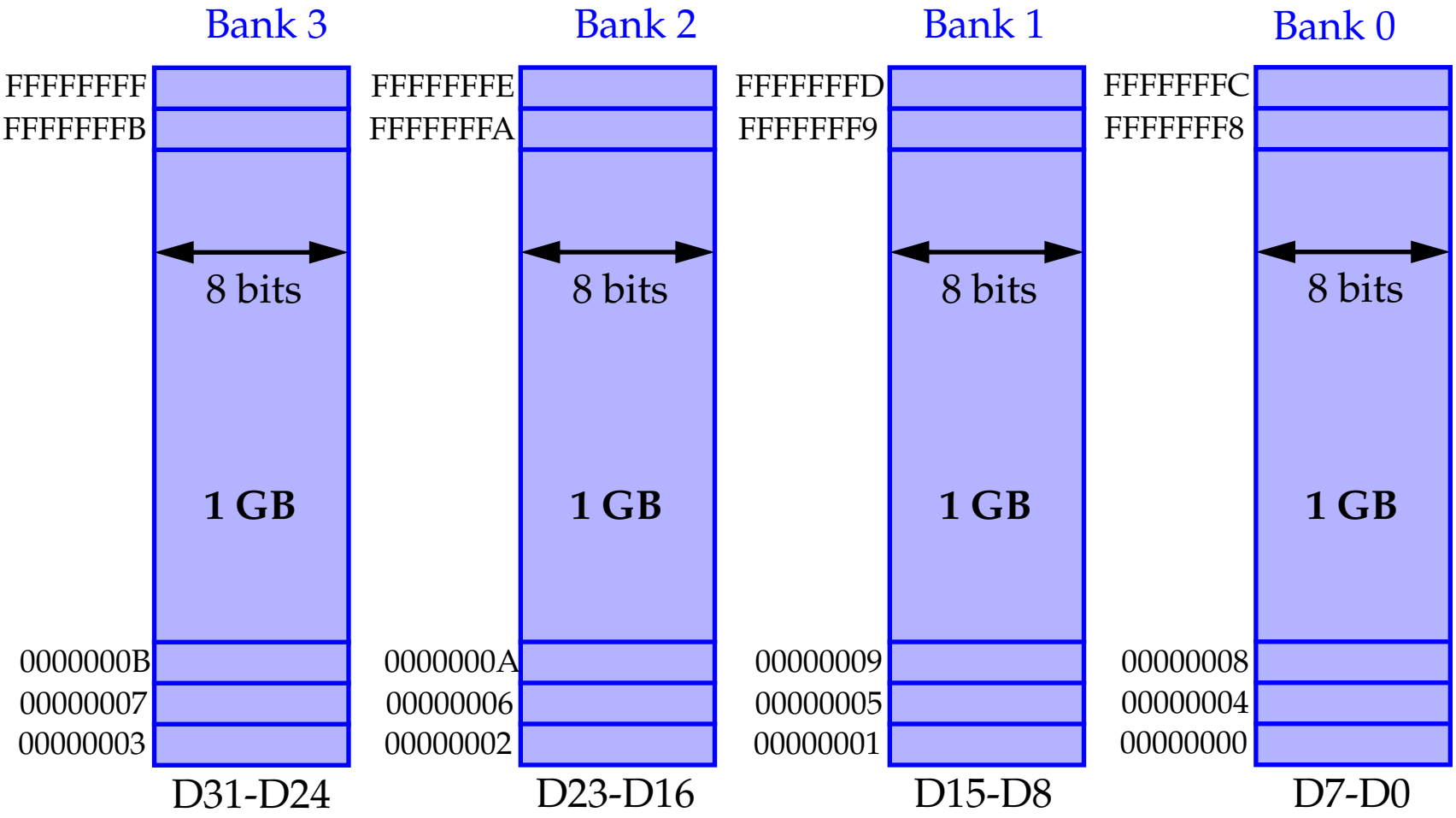
Basic Memory Architecture

Bank layout



Basic Memory Architecture

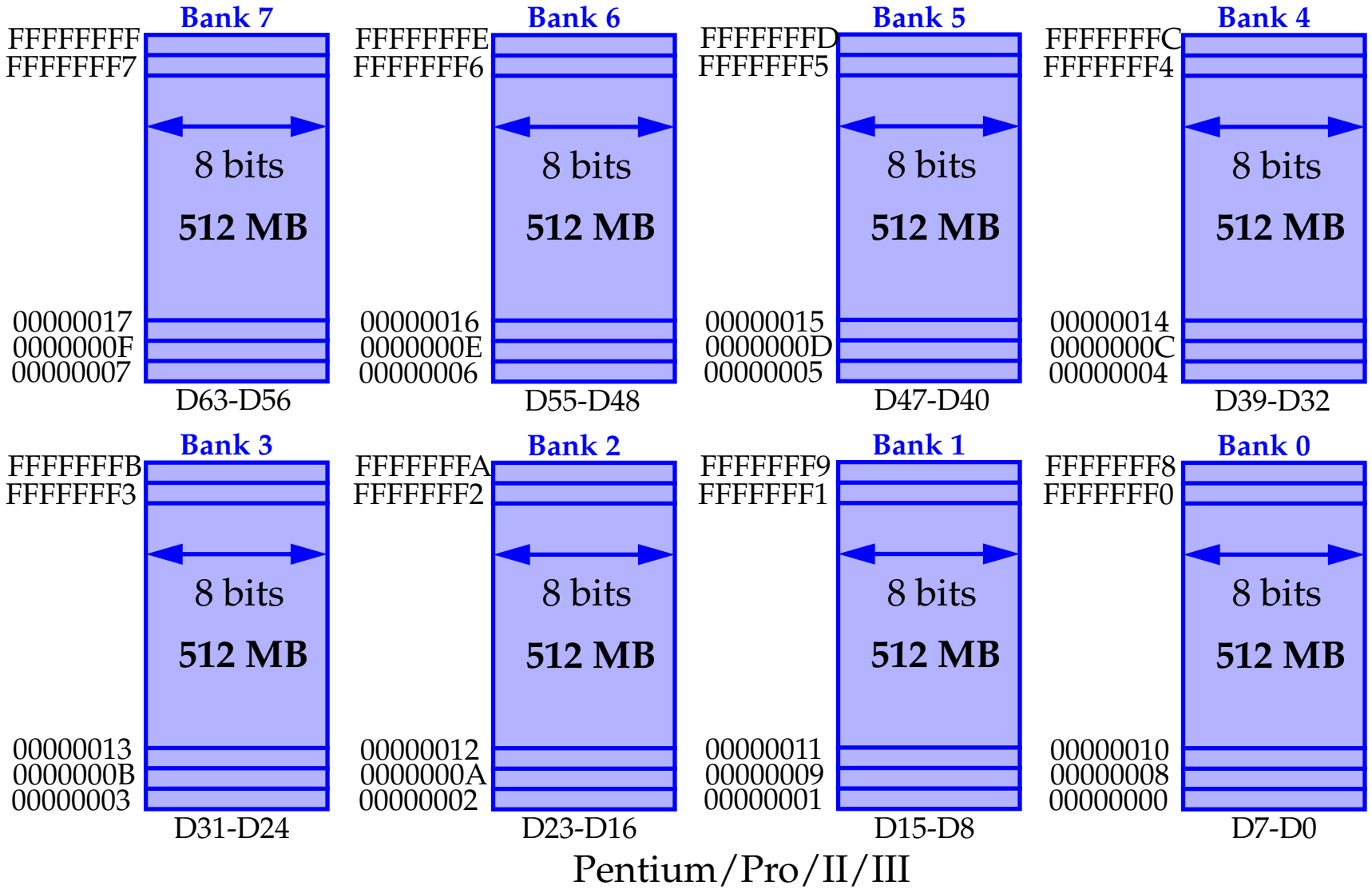
Bank layout



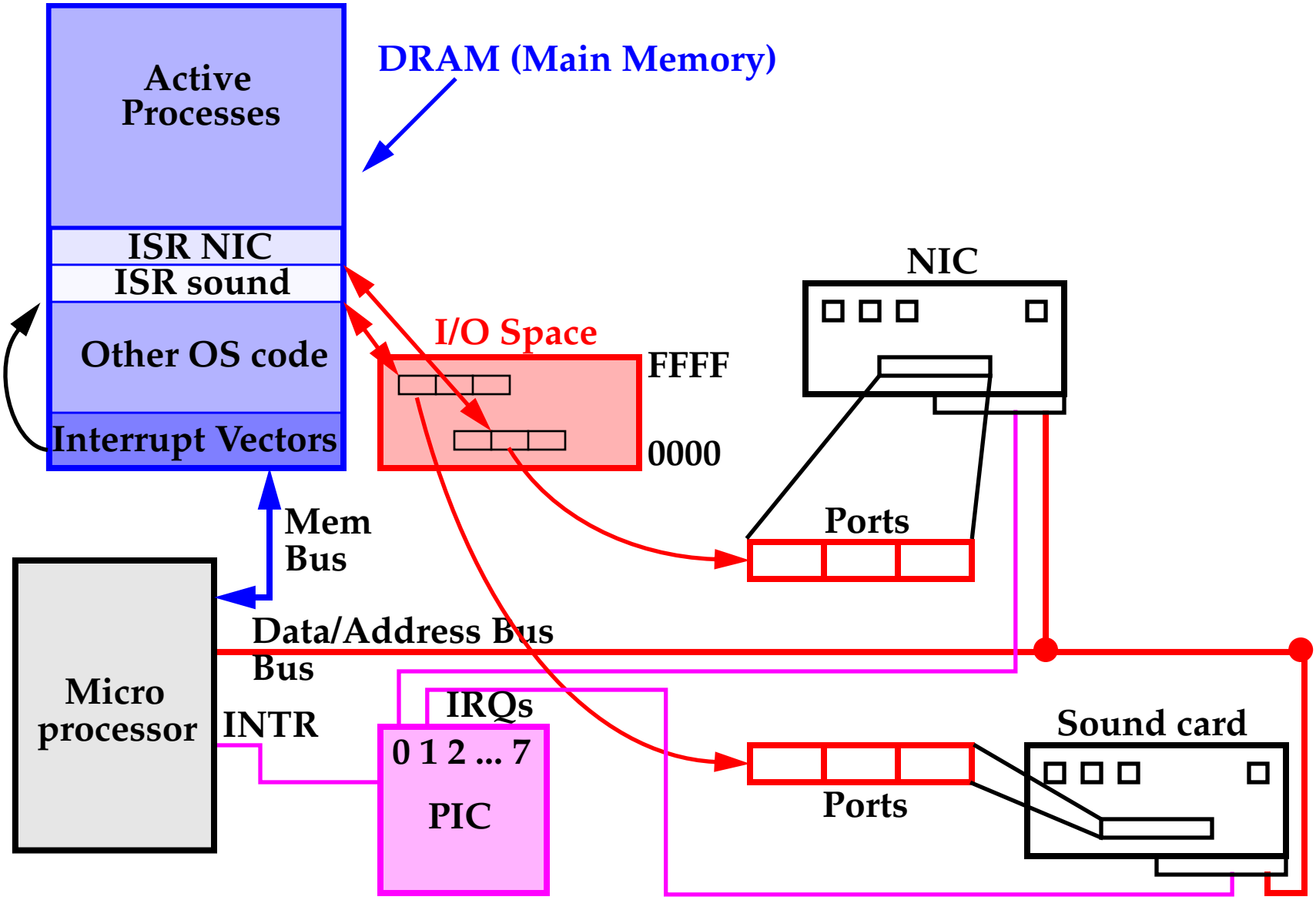
80386DX, 80486

Basic Memory Architecture

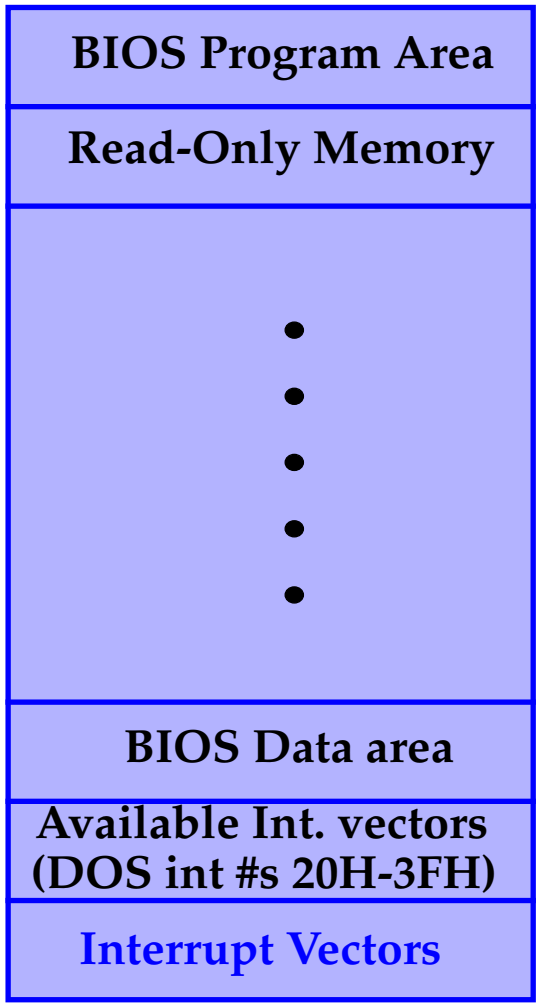
Bank layout



Basic I/O Architecture



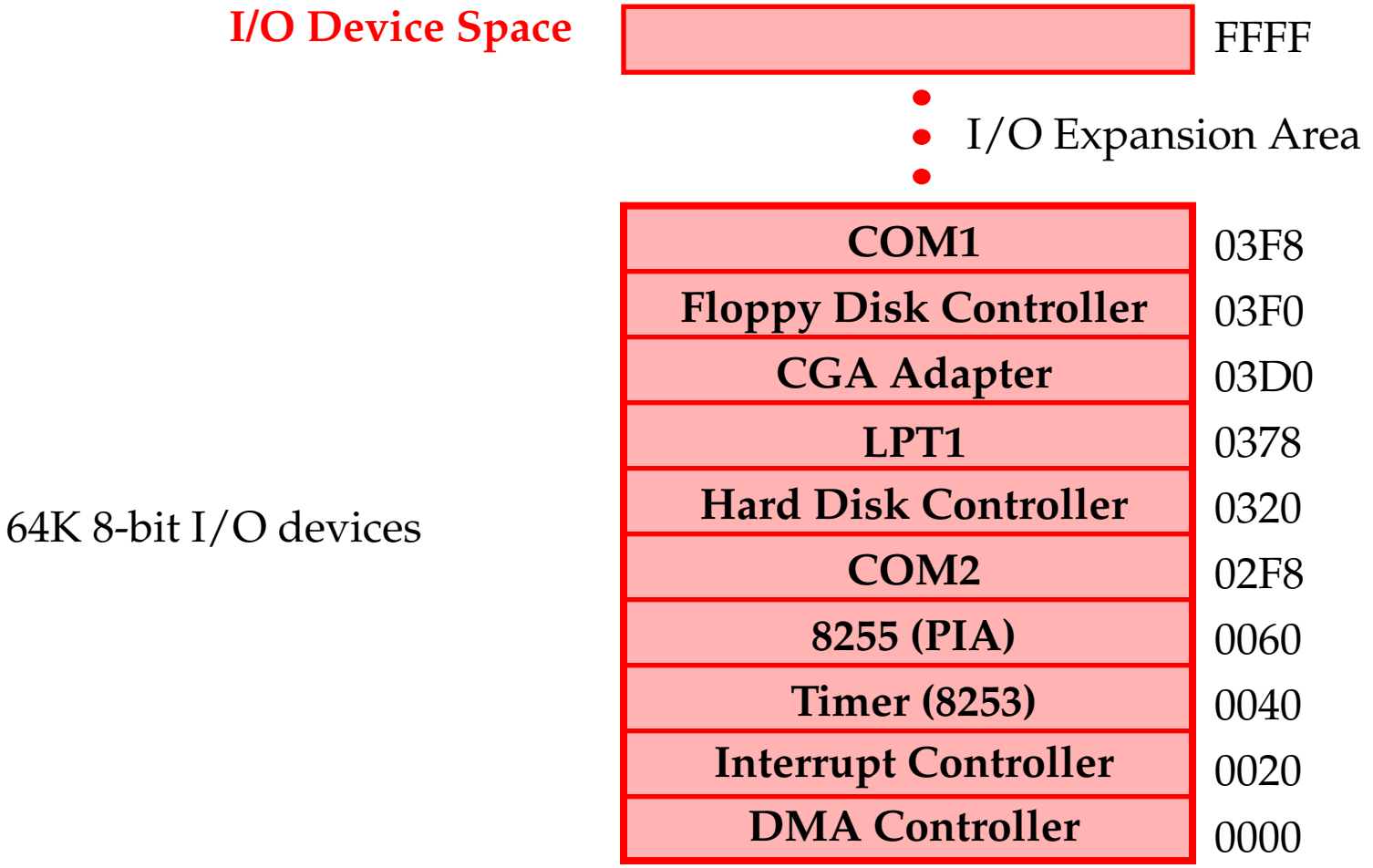
Interrupt Vectors (DOS PC)



Address			Interrupt #	
7C-7F	Video Graphic Chars		1FH	Pts to Data
78-7B	Diskette Parameters		1EH	
74-77	Video Initialization		1DH	
70-73	Timer Tick	(18.2/sec)	1CH	Software Interrupts Synchronous
6C-6F	Keyboard Break		1BH	
68-6B	Time of Day		1AH	
64-67	Bootstrap		19H	
60-63	Resident BASIC		18H	
5C-5F	Printer		17H	
58-5B	Keyboard		16H	
54-57	Cassette		15H	
50-53	Communications		14H	
4C-4F	Diskette/Disk		13H	
48-4B	Memory		12H	
44-47	Equipment Check		11H	
40-43	Video		10H	
3C-3F	Printer		FH	Hardware Interrupts Asynchronous 8259A
38-3B	Diskette		EH	
34-37	Disk		DH	
30-33	Communications		CH	
2C-2F	Communications		BH	
28-2B	Reserved		AH	
24-27	Keyboard		9H	
20-23	Time of Day		8H	
1D-1F	Reserved		7H	
18-1B	Reserved		6H	
14-17	Print Screen		5H	
10-13	Overflow	(CPU)	4H	Microprocessor Interrupts
C-F	Breakpoint	(CPU)	3H	
8-B	Non-maskable	(8087)	2H	
4-7	Single Step	(CPU)	1H	
0-3	Divide by zero	(CPU)	0H	

I/O Space

It is important to notice that these I/O addresses are NOT memory-mapped addresses on the 80x86 machines.



Special instructions (IN/OUT) are used to communicate to the I/O devices.