Programmable Peripheral Interface (82C55)

The 82C55 is a popular interfacing component, that can interface any TTL-compatible I/O device to the microprocessor.

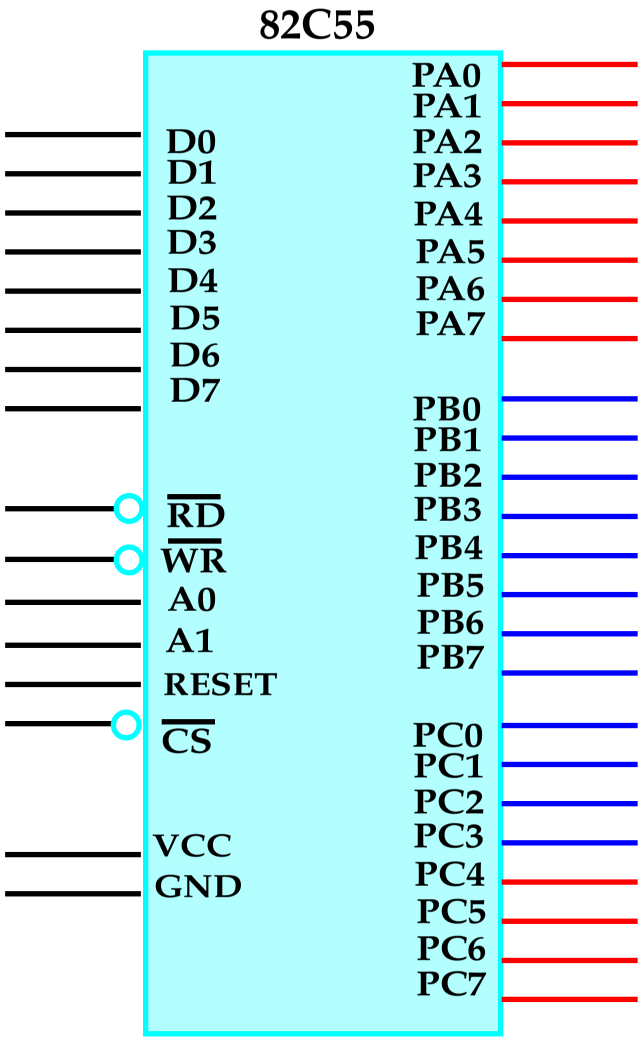
It is used to interface to the keyboard and a parallel printer port in PCs (usually as part of an integrated chipset).

Requires insertion of wait states if used with a microprocessor using higher that an 8 MHz clock.

PPI has 24 pins for I/O that are programmable in groups of 12 pins and has three distinct modes of operation.

In the PC, an 82C55 or its equivalent is decoded at I/O ports 60H-63H.

Pinout of 82C55 PPI



Group A

Port A (PA7-PA0) and upper half of port C (PC7 - PC4)

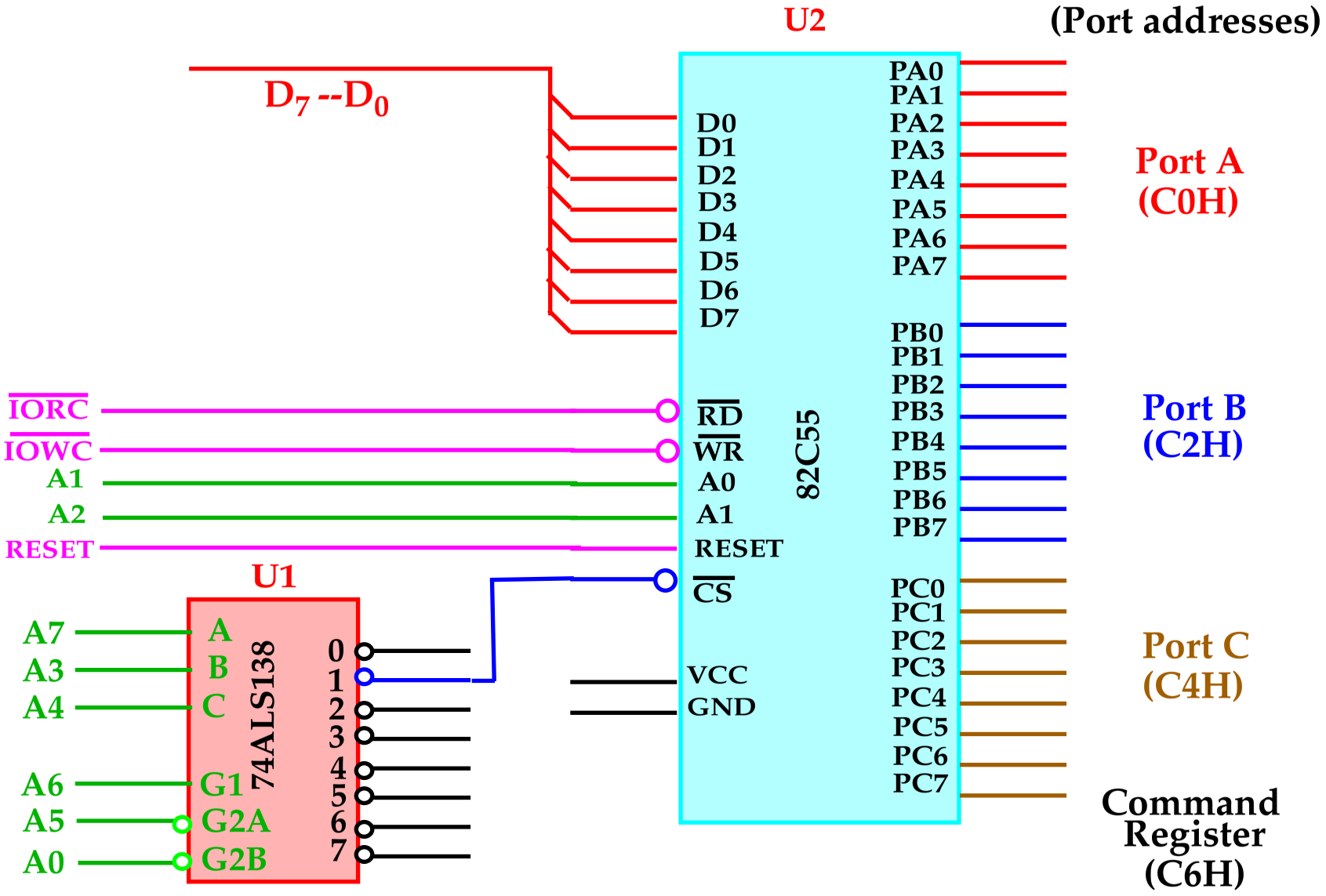
Group B

Port B (PB7-PB0) and lower half of port C (PC3 - PC0)

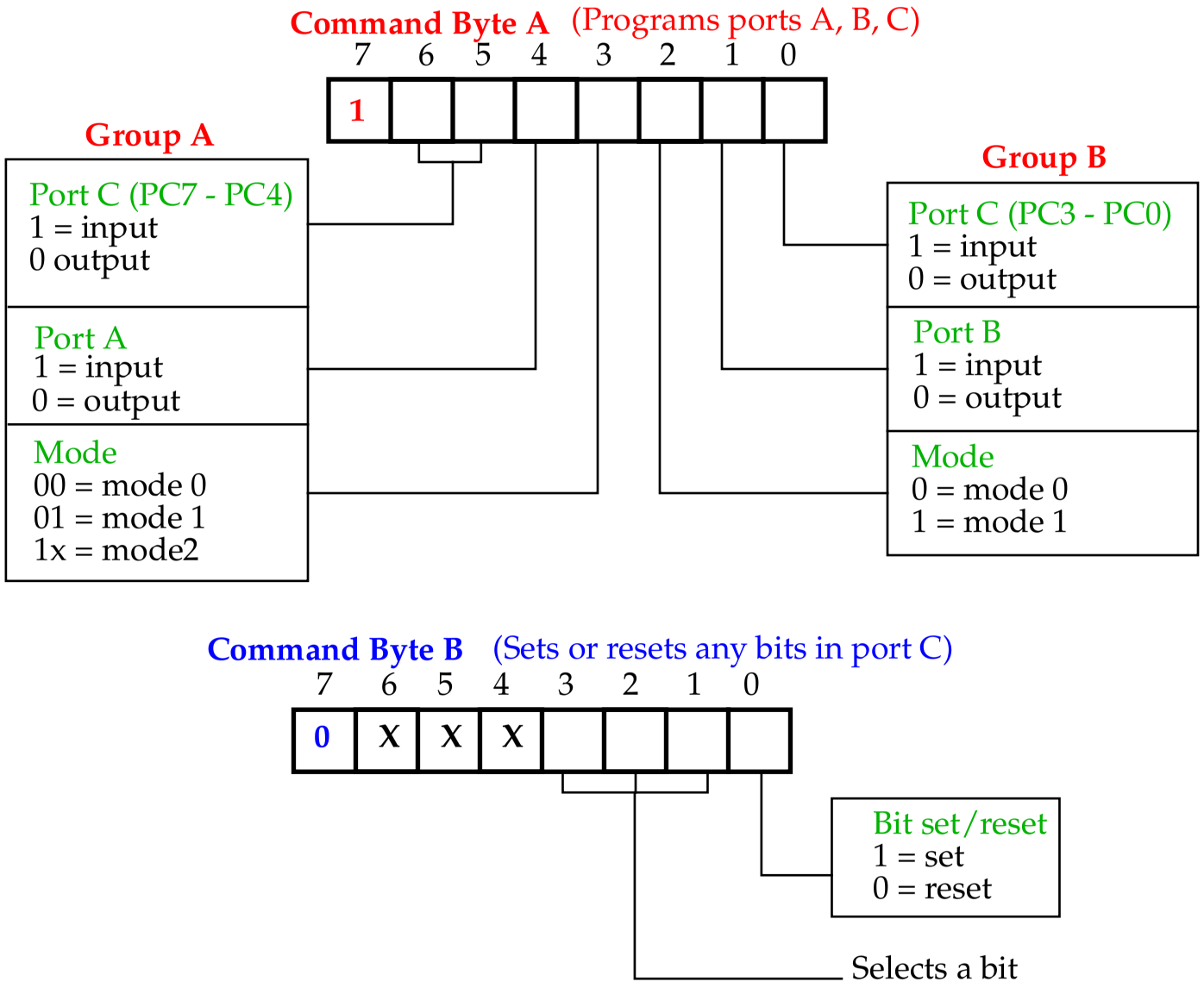
I/O Port Assignments

A_1	A_0	Function
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Command Register

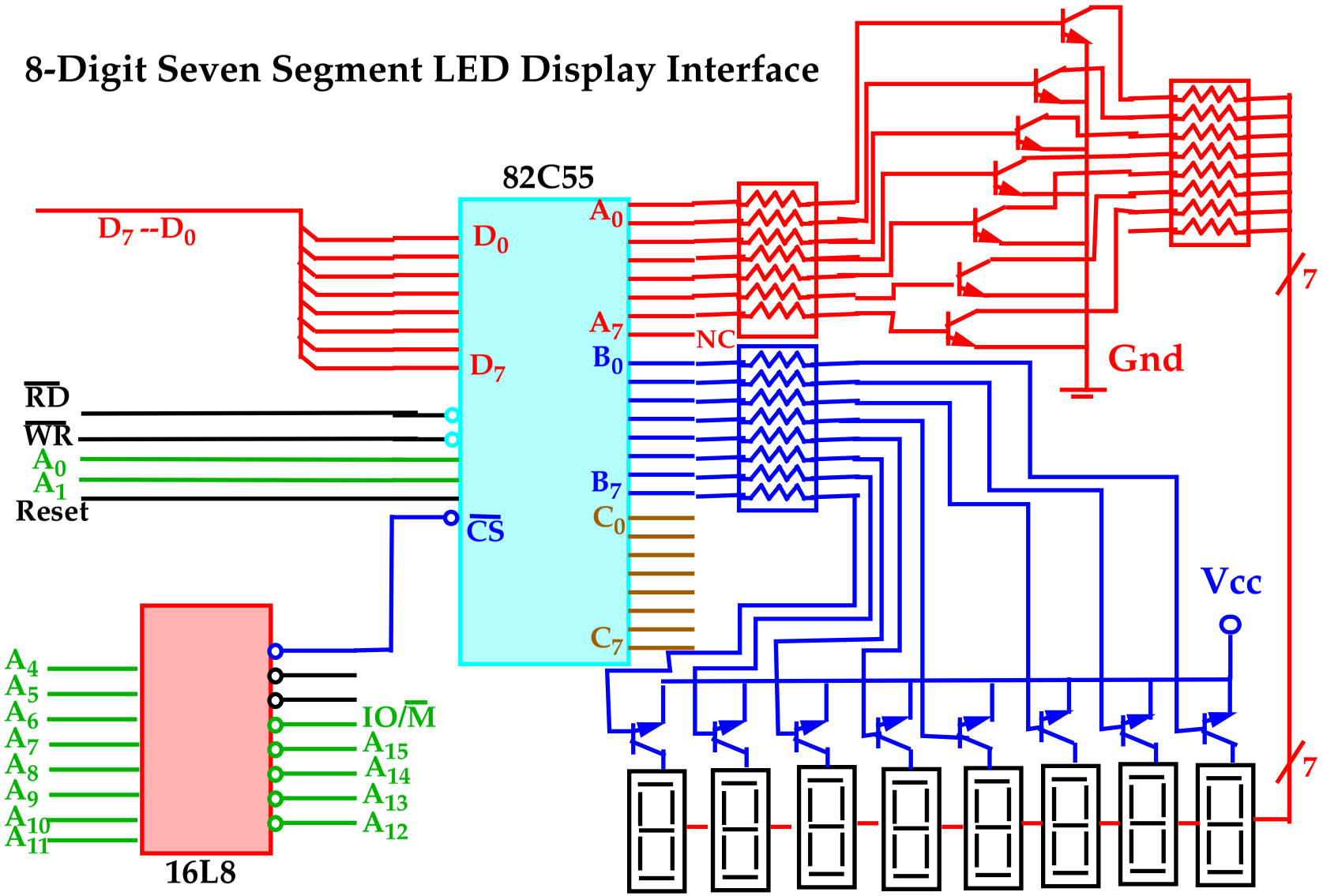
Interfacing the 82C55 PPI



Programming the 82C55



82C55: Mode 0 Operation



82C55: Mode 0 Operation

Mode 0 operation causes the 82C55 to function as a buffered input device or as a latched output device.

In previous example, both ports A and B are programmed as (mode 0) simple latched output ports.

Port A provides the segment data inputs to display and port B provides a means of selecting one display position at a time.

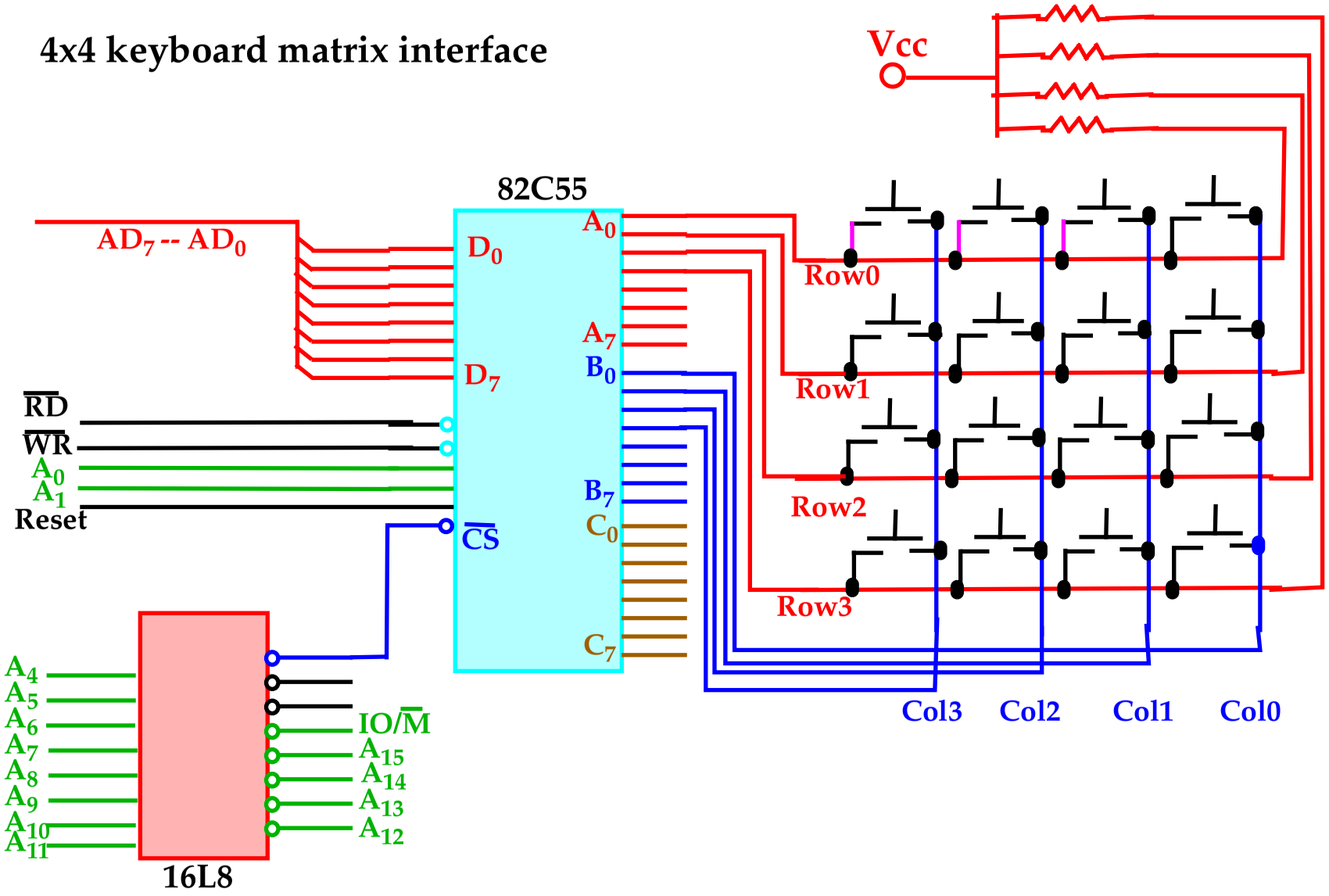
The values for the resistors and the type of transistors used are determined using the current requirements (see text for details).

Textbook has the assembly code fragment demonstrating its use.

Examples of connecting LCD displays and stepper motors are also given.

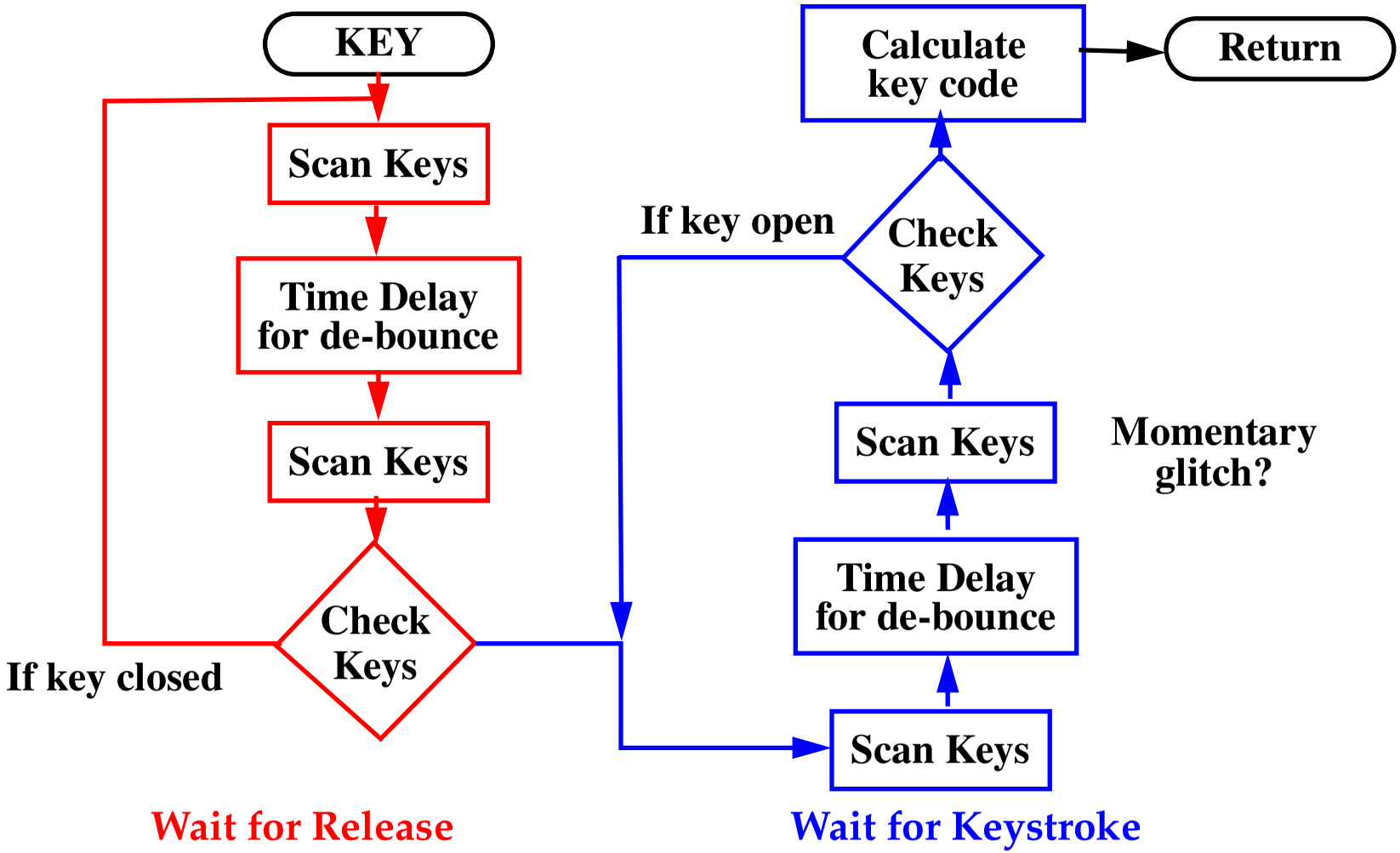
82C55: Mode 0 Operation

4x4 keyboard matrix interface



82C55: Mode 0 Operation

Flow chart of a keyboard-scanning procedure



82C55: Mode 1 Strobed Input

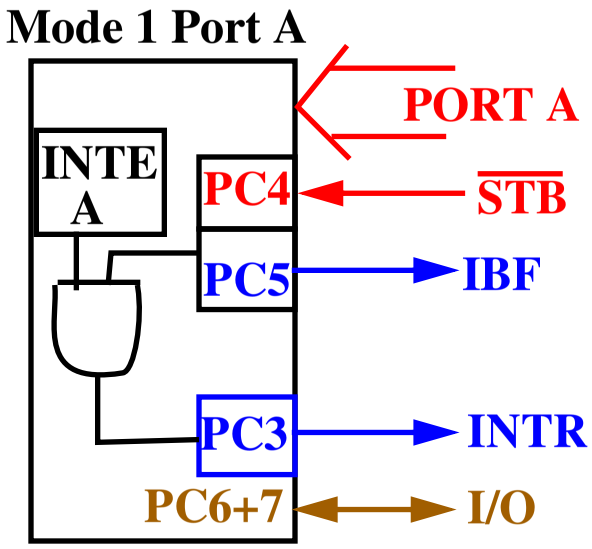
Port A and/or port B function as latching input devices. External data is stored in the ports until the microprocessor is ready.

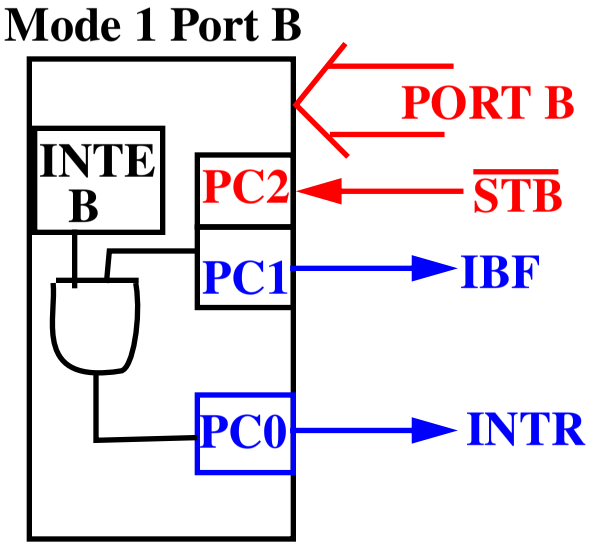
Port C used for control or handshaking signals (cannot be used for data).

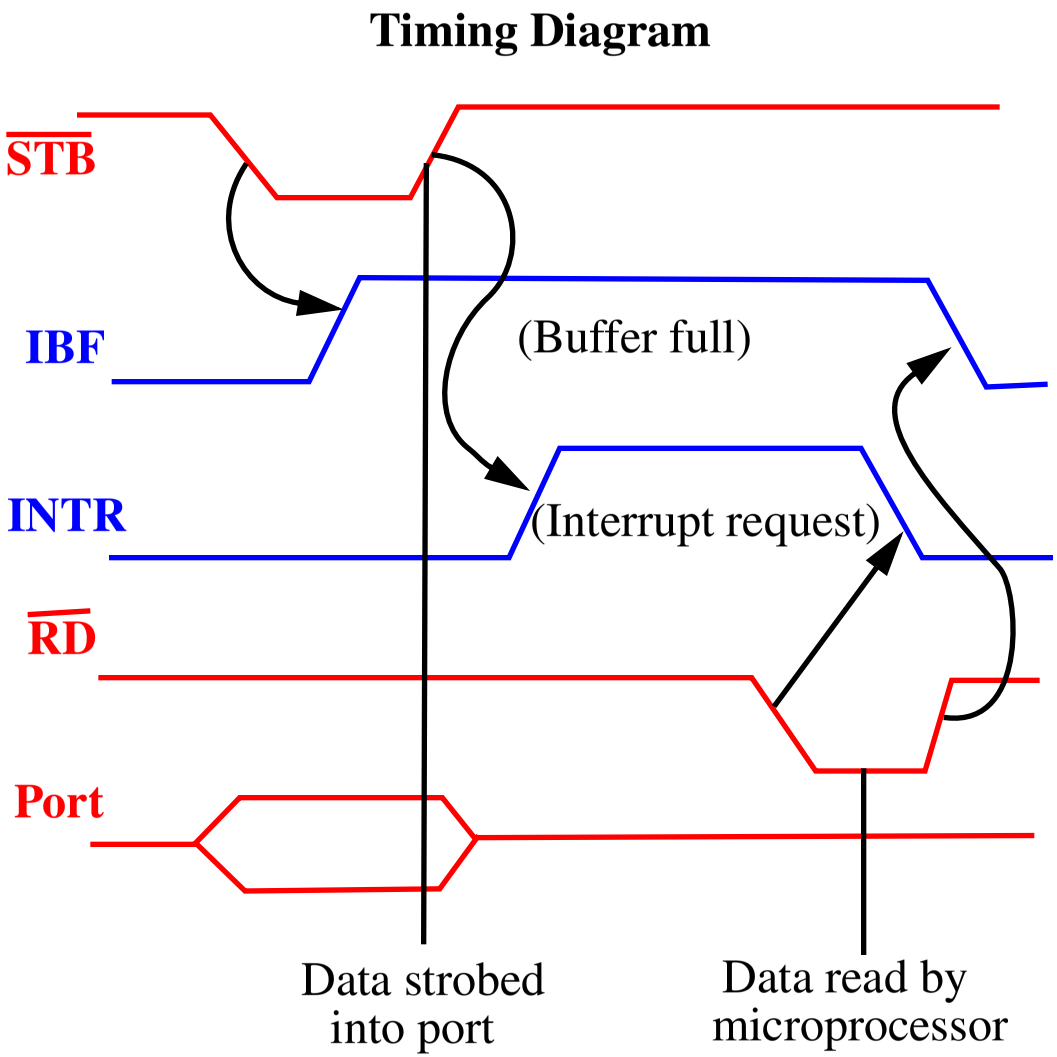
Signal definitions for Mode 1 Strobed Input

$\overline{\text{STB}}$	The strobe input loads data into the port latch on a 0-to-1 transition
IFB	**Input buffer full** is an output indicating that the input latch contain information
INTR	**Interrupt request** is an output that requests an interrupt
INTE	The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC4(port A) or PC2(port B) bits.
PC7,PC6	The port C pins 7 and 6 are general-purpose I/O pins that are available for any purpose.

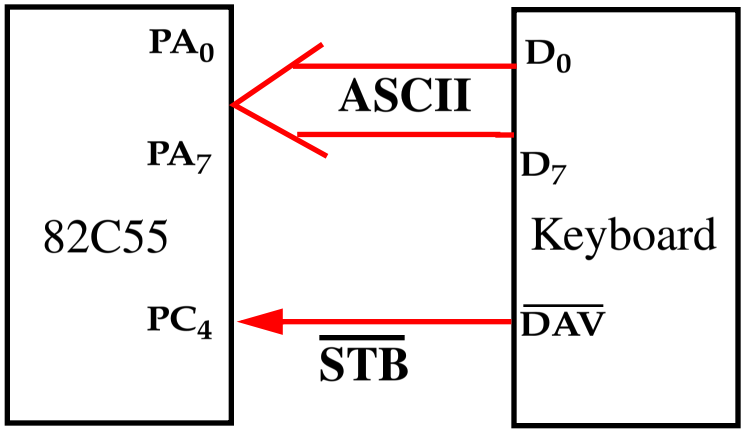
82C55: Mode 1 Strobed Input







82C55: Mode 1 Strobed Input Example



Keyboard encoder debounces the key-switches, and provides a strobe whenever a key is depressed.

DAV is activated on a key press strobing the ASCII-coded key code into Port A.

82C55: Mode 1 Strobed Output

Similar to Mode 0 output operation, except that handshaking signals are provided using port C.

Signal Definitions for Mode 1 Strobed Output

$\overline{\text{OBF}}$ **Output buffer full** is an output that goes low when data is latched in either port A or port B. Goes low on $\overline{\text{ACK}}$.

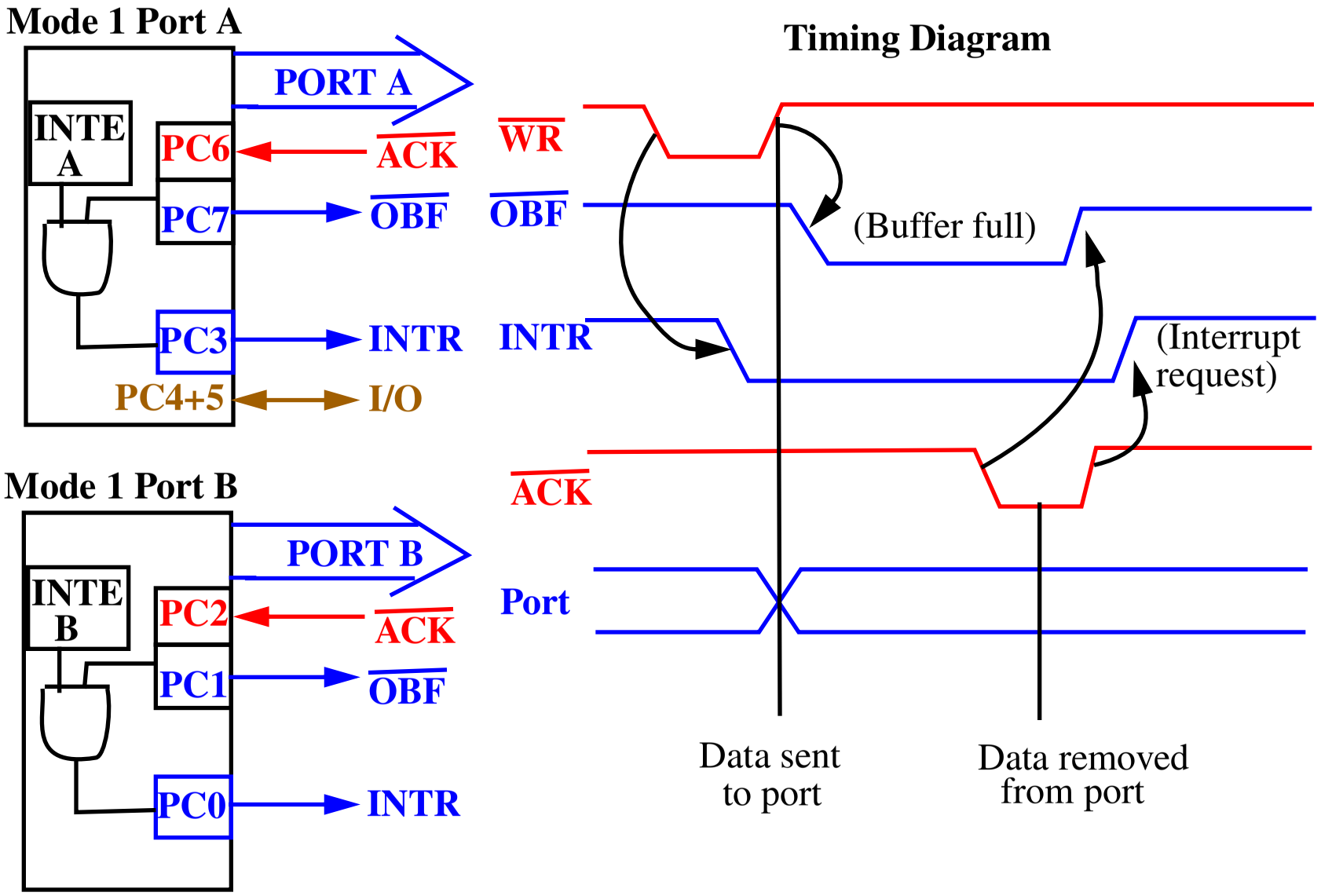
$\overline{\text{ACK}}$ The **acknowledge** signal causes the $\overline{\text{OBF}}$ pin to return to 0. This is a response from an external device.

INTR **Interrupt request** is an output that requests an interrupt

INTE The **interrupt enable signal** is neither an input nor an output; it is an internal bit programmed via the PC6(port A) or PC2(port B) bits.

PC5,PC4 The port C pins 5 and 4 are general-purpose I/O pins that are available for any purpose.

82C55: Mode 1 Strobed Output

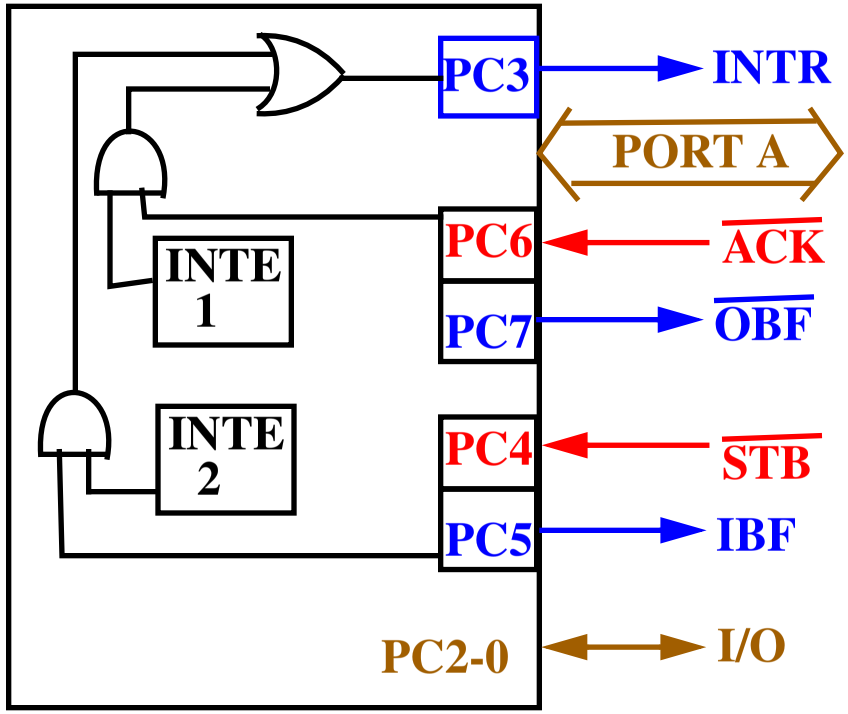


82C55: Mode 2 Bi-directional Operation

Only allowed with port A. Bi-directional bused data used for interfacing two computers, GPIB interface etc.

INTR	**Interrupt request** is an output that requests an interrupt
$\overline{\text{OBF}}$	**Output buffer full** is an output indicating that the output buffer contains data for the bi-directional bus
$\overline{\text{ACK}}$	**Acknowledge** is an input that enables tri-state buffers which are otherwise in their high-impedance state
$\overline{\text{STB}}$	The strobe input loads data into the port A latch
IFB	**Input buffer full** is an output indicating that the input latch contains information for the external bi-directional bus
INTE	**Interrupt enable** are internal bits that enable the INTR pin. Bit PC6(INTE1) and PC4(INTE2)
PC2,PC1 and PC0	Theses port C pins are general-purpose I/O pins that are available for any purpose.

82C55: Mode 2 Bi-directional Operation



Timing diagram is a combination of the Mode1 Strobed Input and Mode 1 Strobed Output Timing diagrams.