Cadence Capture CIS

Capture CIS is an EDA (Electronic Design Automation) tool. It is frequently used to create a schematic design for **PCB (Printed Circuit Board) and FPGA project**. The simple steps involved in schematic design include placing and connecting part, running Design Rules Check, and generating netlist. The tool is also capable of functional and timing simulations for FPGA project, board level simulation for PCB project and analog/mixed signal simulation using PSpice.

This tutorial is the first of two parts in PCB project tutorial and will cover all basic steps involved in creating a schematic netlist for PCB layout design (for layout design tutorial see Layout Plus Tutorial).

For more information about Capture CIS, please refer to Capture Knowledge System (From Capture CIS main menu, go to Help → Capture CIS Help → Capture Help)

Open Capture CIS

From Windows Start Menu, select **Program → Cadence PSD 15.0 → Capture CIS**. You will see Studio Suite Selection dialog box (Figure 1), choose PCB Design Studio with Capture CIS

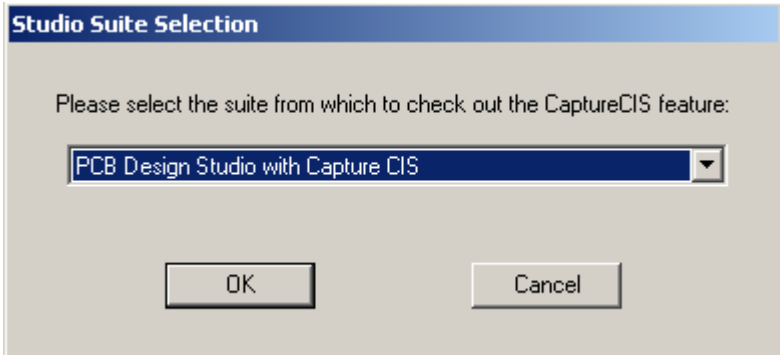

Figure 1: Studio Suite Selection Dialog

Create a new project by going to File → New → Project. Enter project name, select **schematic** project type and enter location you want the project to be saved as shown in Figure 2. (You might want to save on your network drive if you're running Capture CIS in campus's laboratory)

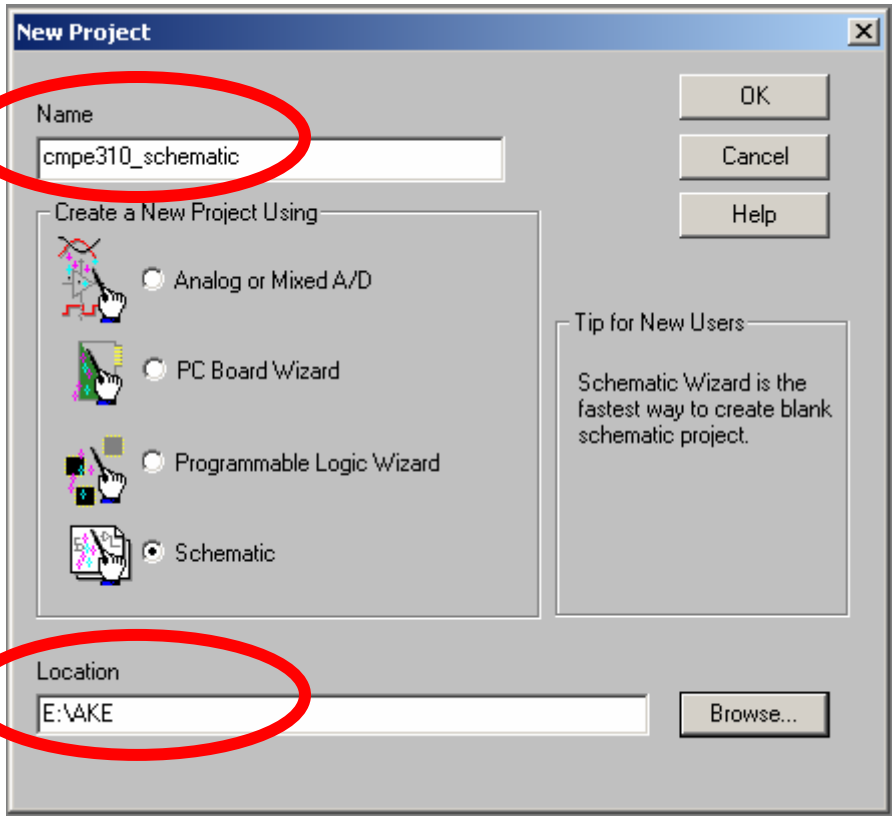

Figure 2: New Project Dialog

Capture CIS will create new schematic for PCB project and you will see your project workspace as shown in Figure 3.

Tips:

- You can create a new schematic page by right click on the schematic folder on project window and select **New Page**.
- Main menu (on the top) is changed according to an active window, every time you click on the particular windows (project window, schematic page window or session log window). If you can't find some options, it might be because you got the wrong window as the active window.

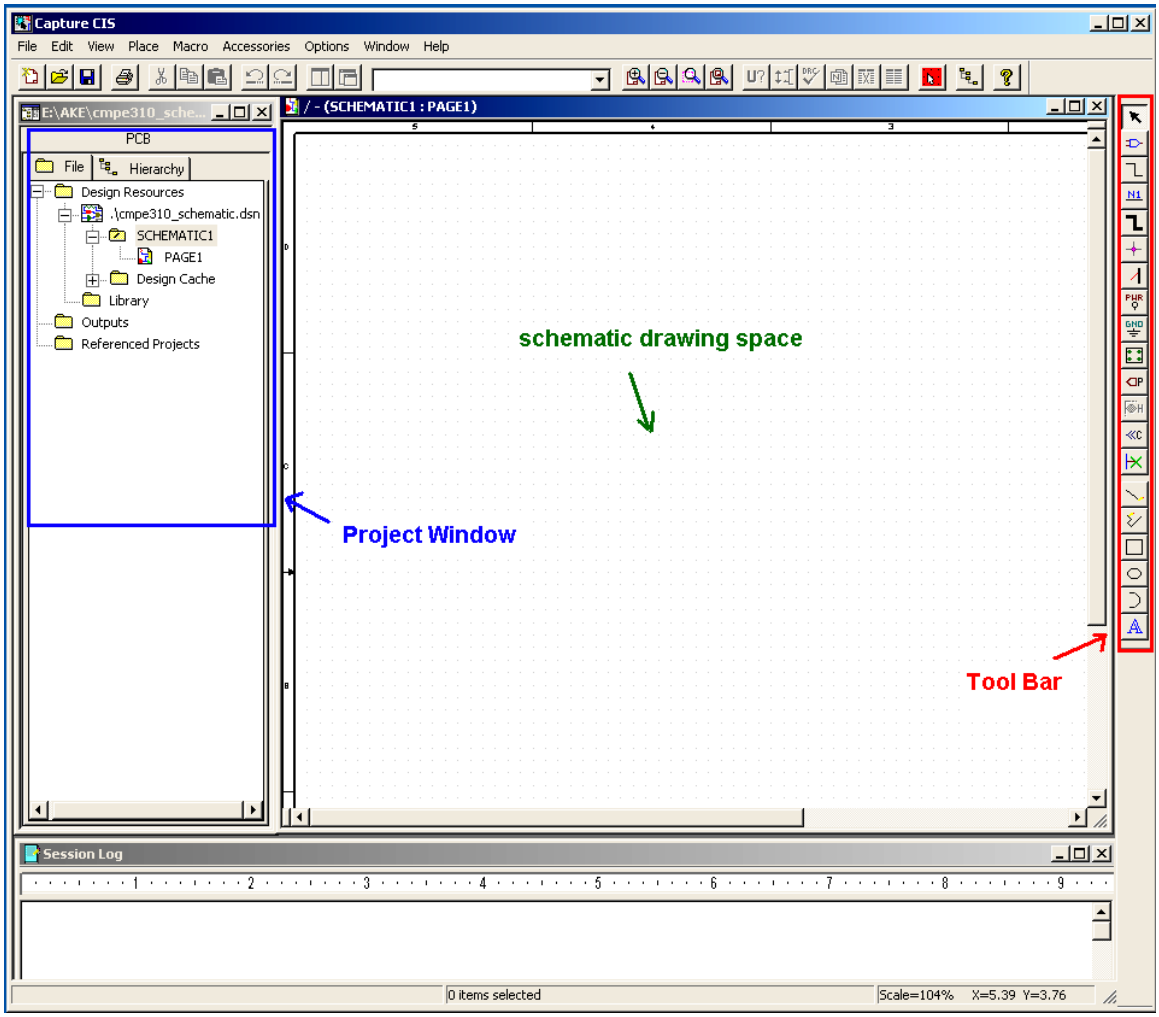

Figure 3: Schematic Project Workspace

Placing Part

You can place the circuit components of your board by click on CIS main menu; **Place → Part** (make sure the schematic window is the active window). Figure 4 shows the Place Part Dialog Box; you can search for a part through libraries by typing on Part textbox. You can select one particular library to be listed/searched or select multiple libraries at a time. Some part has multiple packages on the same chip (ex. 74LS10 has 3 packages of 3-input NAND gate), Capture CIS will automatically place all packages on the same chip before place a new chip (ex. you will see the instance of part as U1A, U1B for the package A and B of instance U1).

Highlight the part you want to place on schematic and click OK. Click on the schematic work space to place the part, you can place same part multiple times, press ESC to end the command. Figure 5 shows the example of placing parts on the schematic.

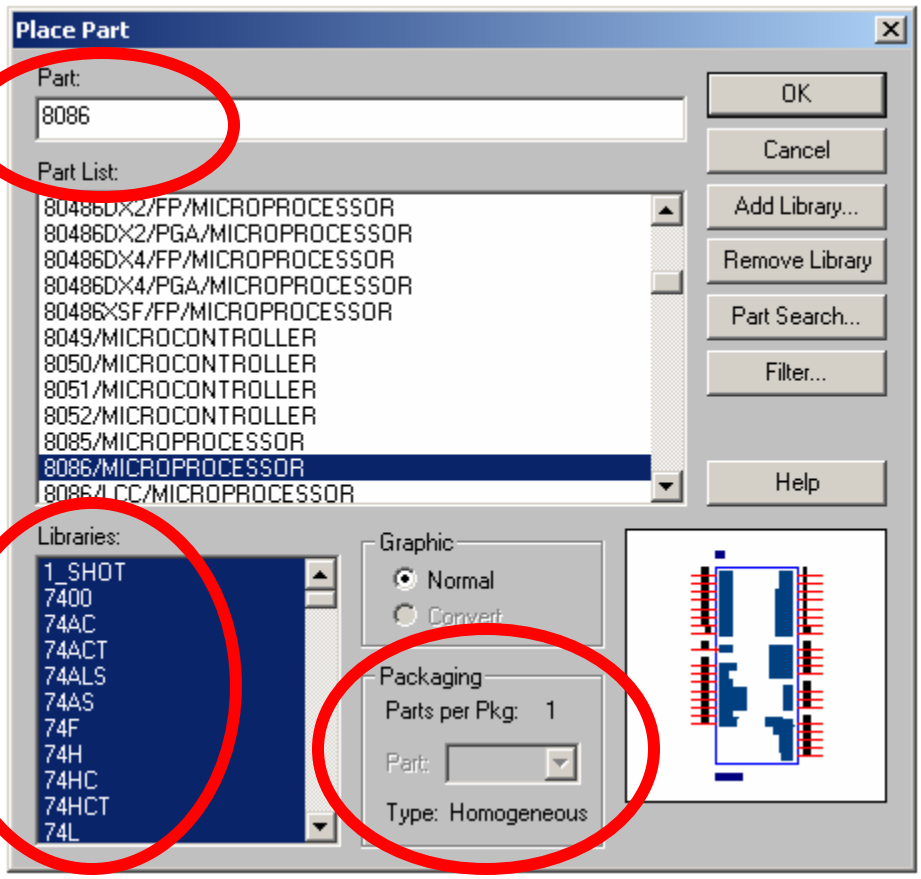

Figure 4: Place Part Dialog

Tips:

- Easy access to **Place Part** by clicking on  button on the toolbar or press **Shift+P**.

More info:

- Capture CIS provides another way to collect parts using a database instead of part library. If you have a part database setup, go to **Place → Database Part**. However, we do not have part database setup for cmpe310 class.
- Another cool way to find the part if you don't have it on local library or database is to search through **ActiveParts project**, a free online electronic part database. To use this feature, you need to have access to the internet and have Internet Component Assistant (ICA) setup. For cmpe310 class, you have all parts you'll need for the project setup for you on the local library. (see how nice we are!)

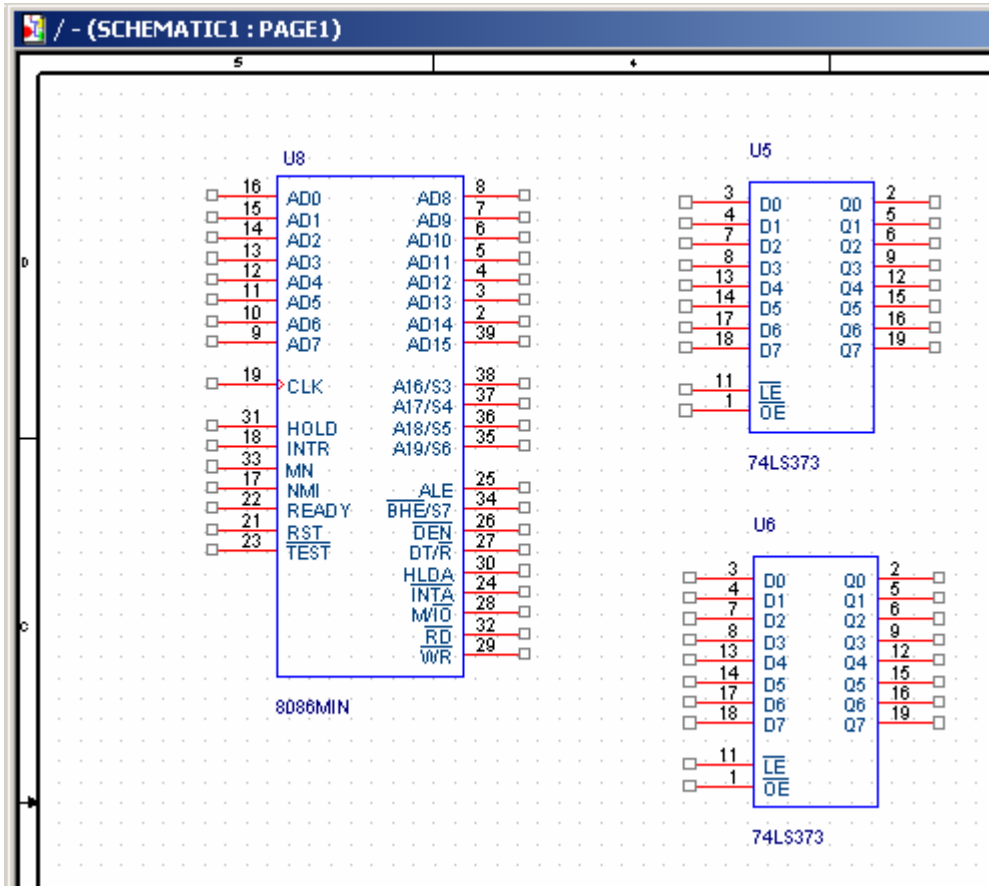

Figure 5: Place part example

Placing Power Source

To place power source on the schematic, simply go to **Place → Power** on the main menu. Select **CAPSYM** library and then use either **VCC or GND** for your power sources as shown in Figure 6. Click OK and then click on the schematic to place power source.

Tips:

- Easy access to **Place Power** by clicking on  button on the toolbar or press **Shift+F**.
- Place Power and Place Ground on the main menu actually look for power sources on the same set of libraries, you can use either one of them to find VCC or GND
- For multiple supply voltages design, you can **change the Power name to distinguish between power domains**. (ex. VCCA, VCCD, GNDA and GNDD for analog and digital power domains)

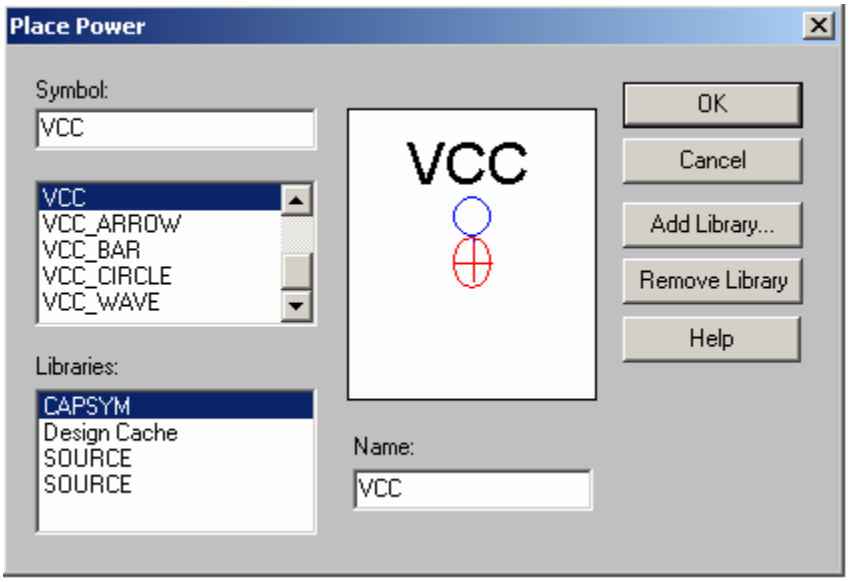

Figure 6: Place Power Source

Connecting Part

There are many ways to connect parts on your schematic; this tutorial will go over some of them that are enough to make a simple PCB design.

On-Page Connection: Connect parts on the same page

Place Wire: The easiest way to connect part is to use a wire. Go to **Place → Wire** and then click once on the starting point of the connection. Move the mouse to the destination point (you might need to click along the way to make a 90 degree turn). Make sure you do not cross the wire to existing connections; Capture CIS will give you a warning (**red dot with ⚠ sign**) whenever 2 nets are about to be connected. Double click to end the wire.

Tips:

- Zoom in to the part you're making a connection to make sure that you got them connected in the right place.
- Press **"I" for zoom-in and "O" for zoom-out**, the center of zooming is the position of the mouse. These shortcuts make it's very easy to work on your design.
- Again, easy access to **Place Wire** by clicking on button on the toolbar or press **W**.

Place Net Alias: Sometime, making all wire connections on your schematic will make your design looks really messy and confusing. Another way to make on-page connection is to use net alias. Net Alias can be place **on a wire or bus**, simply go to **Place → Net Alias** and then type net name you want to assign to a net as shown in Figure 7. After click OK, click on a wire or bus that you want to make net alias. Press ESC to end the command.

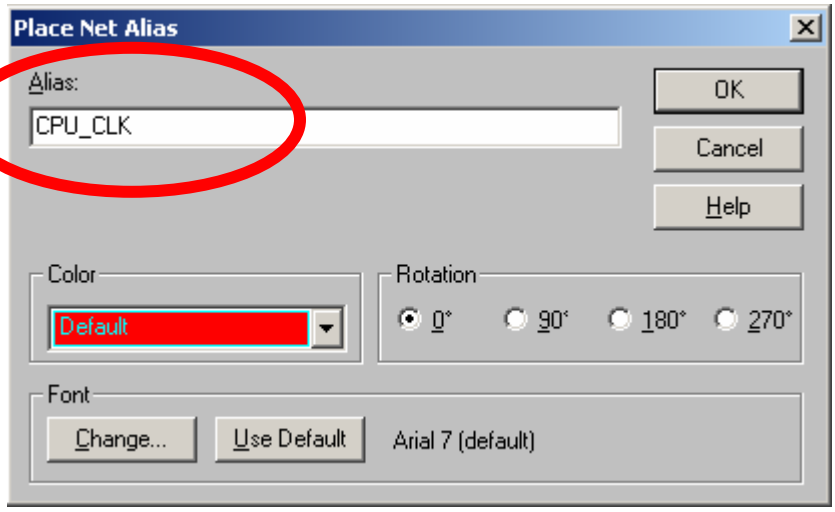

Figure 7: Place Net Alias

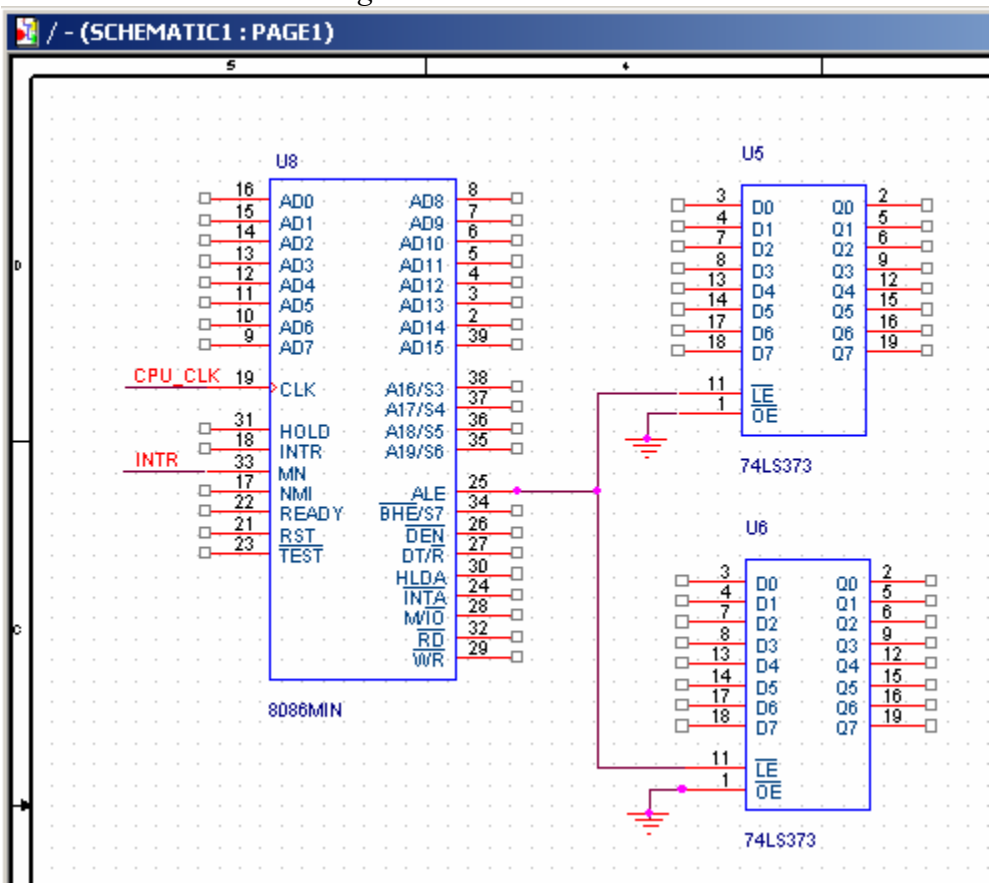

Figure 8: An example of net connections using wires and net aliases.

Figure 8 shows an example of net connections on the schematic using wires and net aliases.

Tips:

- Easy access to **Place Net Alias** by clicking on  button on the toolbar or press **N**.
- You can place multiple net aliases at a time, Capture CIS will **automatically change net name** for you appropriately, if the first net alias is named D0, the next net alias will automatically be D1, D2, D3 and so on. This help you make net aliases very fast especially with buses.

Place Bus: To make connections look cleaner, you can make a bus on your schematic by go to **Place → Bus** on the main menu. Click on the start and end point to make a bus the same way as making a wire. You'll need to leave a space between a bus and pins for bus entries and wires. Next, create net alias for your bus, the format for bus alias is a string followed by **[s:e]** where **s** is the bit position of the first net and **e** is the bit position of the last net. For example, if you want to make a 16-bit address bus called A, you can name it as A[0:15] or A[15:0] (both of them are valid). Now you'll need to make a bus entry to connect between a wire and a bus (**you cannot connect bus entry directly to a pin, Capture CIS requires bus, bus entry and wire to make a pin-to-bus connection**). Go to **Place → Bus Entry** on the main menu and then click on the points along the bus you want to have entries. After placing all bus entries you need, now place a wire connect between each bus entry to a pin or net. The last step is to make net aliases for all the nets connected to the bus, the net name need to be the same name as your bus alias except there are **no square bracket [..]**, you'll need to put the number appropriate to the bit position of the bus you want to connect to. For example, if you want a particular net to be connected to bit 3 of address bus A, you'll make net alias as A3. Figure 9 shows all the steps required making bus connections and Figure 10 shows an example of making on-page connections using wires, net aliases, and buses.

Tips:

- Easy access to **Place Bus** or **Bus Entry** by clicking on  or  button on the toolbar or press **B** or **E**.
- If you want to check the connection on a particular net, right click on the net and click "**select entire net**". Capture CIS will **highlight all connections on that net**.
- It is **faster to make only one complete bus connection (bus entry, wire and net alias), and then copy it** to make other connections. (As explain earlier, Capture CIS will automatically change net name to appropriate name). First, select a group of bus entry, wire and net alias then hold CTRL key while click once on the group and then move your mouse to the location you want a copy of bus connection to be placed. (This trick will be shown in class)

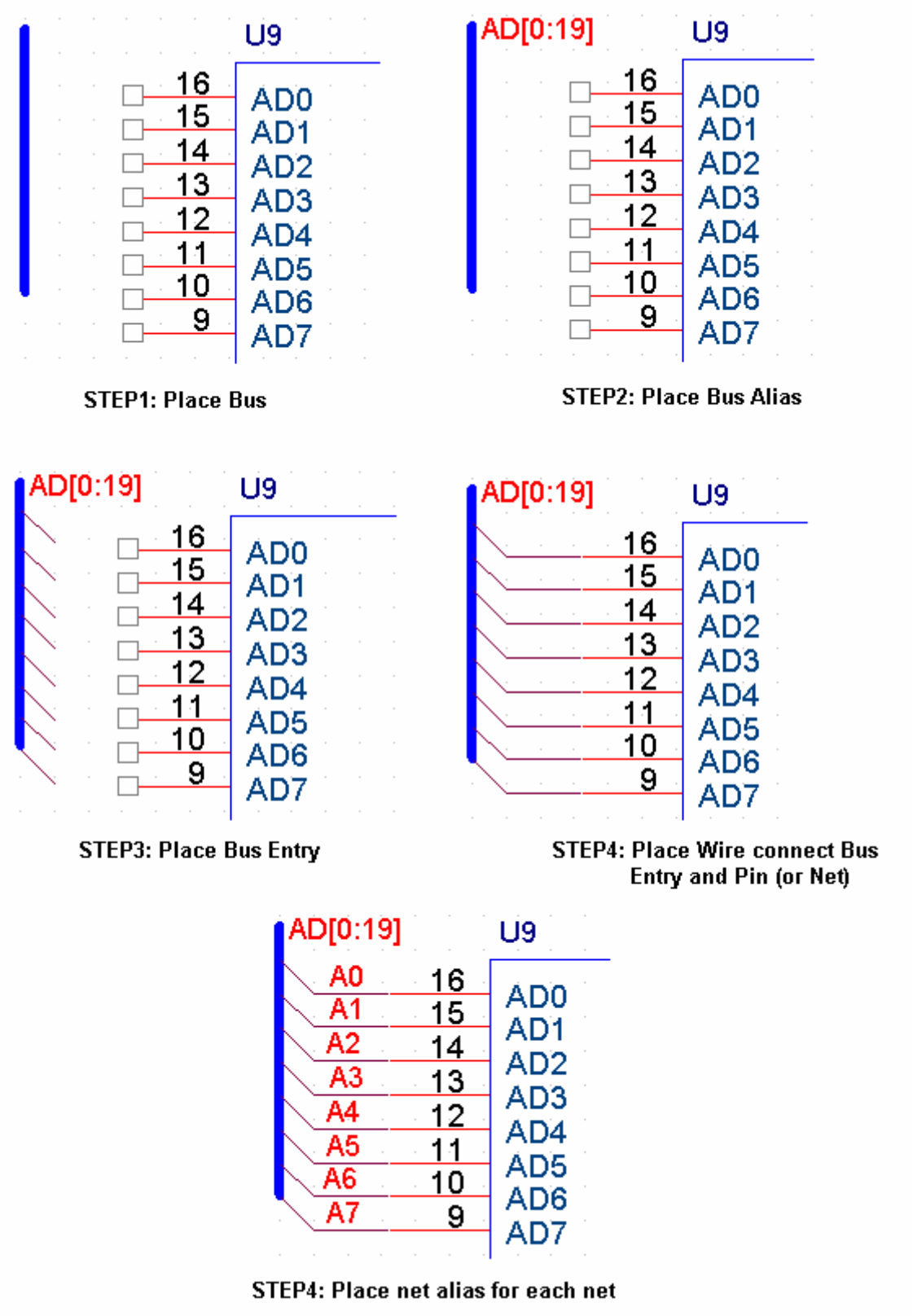

Figure 9: Steps involved in making bus connections

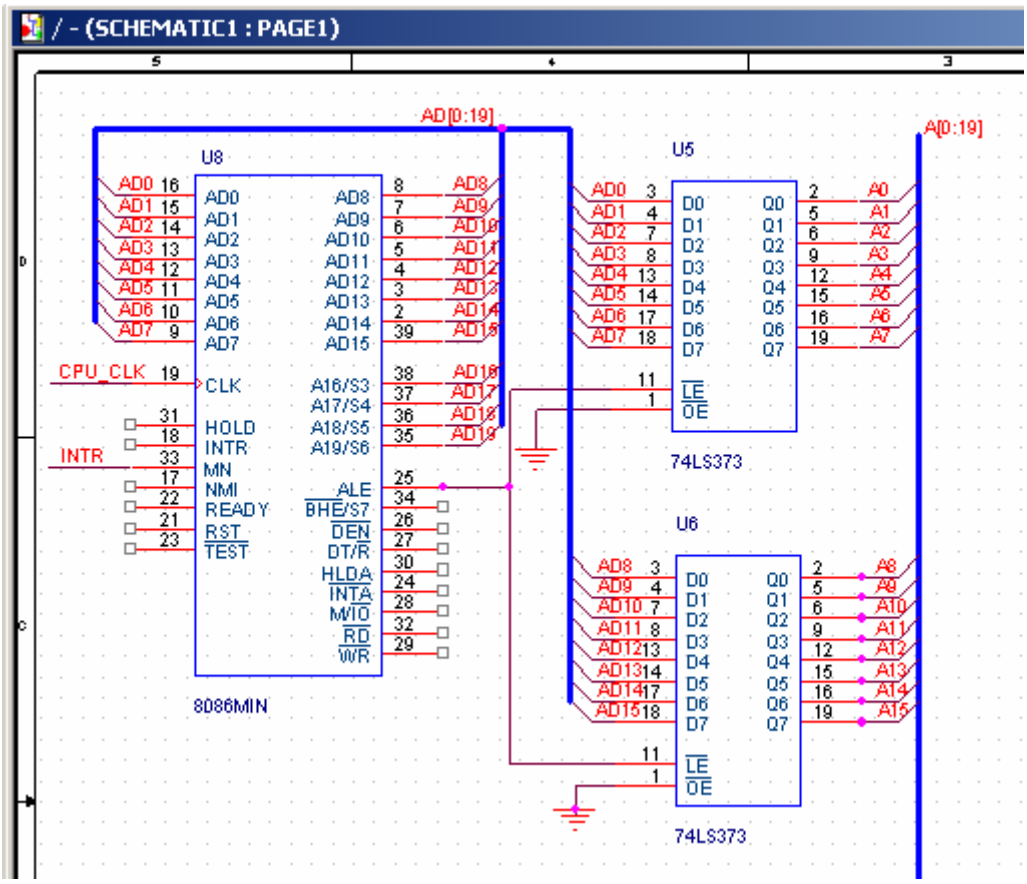

Figure 10: An example of making on-page connections.

Off-Page Connection: Connect parts between pages

Capture CIS provides an off-page connector for this task. To create off-page connector, go to **Place → Off-Page Connector** on the main menu. Use either **OFFPAGELEFT-L or OFFPAGELEFT-R** from **CAPSYM** library, change a name of connector to the name you like as shown in Figure 11. You can place off-page connectors anywhere on the schematic and then connect a net to the off-page connector.

Tips:

- Easy access to Place Off-Page Connector by clicking on  button on the toolbar.
- Making all inputs of your schematic page in the same direction and do the same for the outputs (OFFPAGELEFT-L vs. OFFPAGELEFT-R) will help your design easier to be read.

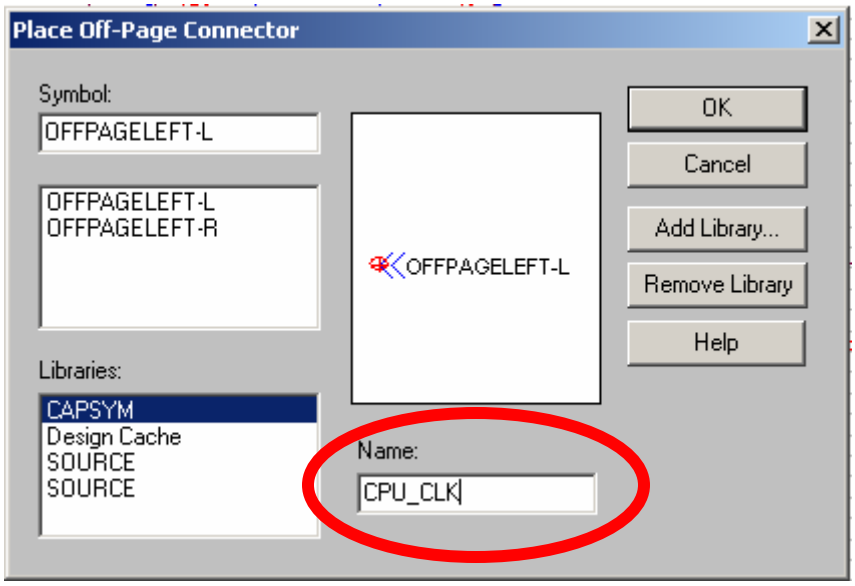

Figure 11: Place Off-Page Connector

No Connection

Capture CIS will complain if there are input pins of the part with no connection when you run Design Rules Check (does not complain for output pins). It is a **good practice to mark these no connection pins** including outputs so that you do not forget to connect some important pins on your design.

To place a no connect mark, go to **Place → No Connect** and then click on the pin that has no connection.

Tips:

- Easy access to **Place No Connect** by clicking on button on the toolbar or press **Shift+X**.

Design Rules Check (DRC)

Running **DRC** help verify your design by checking for open connection, floating off-page connector and so on. However, it is not a magical tool. It does not know if you make a wrong connection on your design such as connect the wrong bus to the wrong pin or connect VDD supply to GND pin.

To run DRC, click on schematic folder on the project window and then go to **Tool → Design Rules Check**. Check on "**View Output**" option on the bottom of the dialog to see the report after DRC run (Figure 12). You can modify other options but for most of the time, default options work very well. Now, click OK button, sit and relax. Take a look at the DRC report and fix errors if there are any.

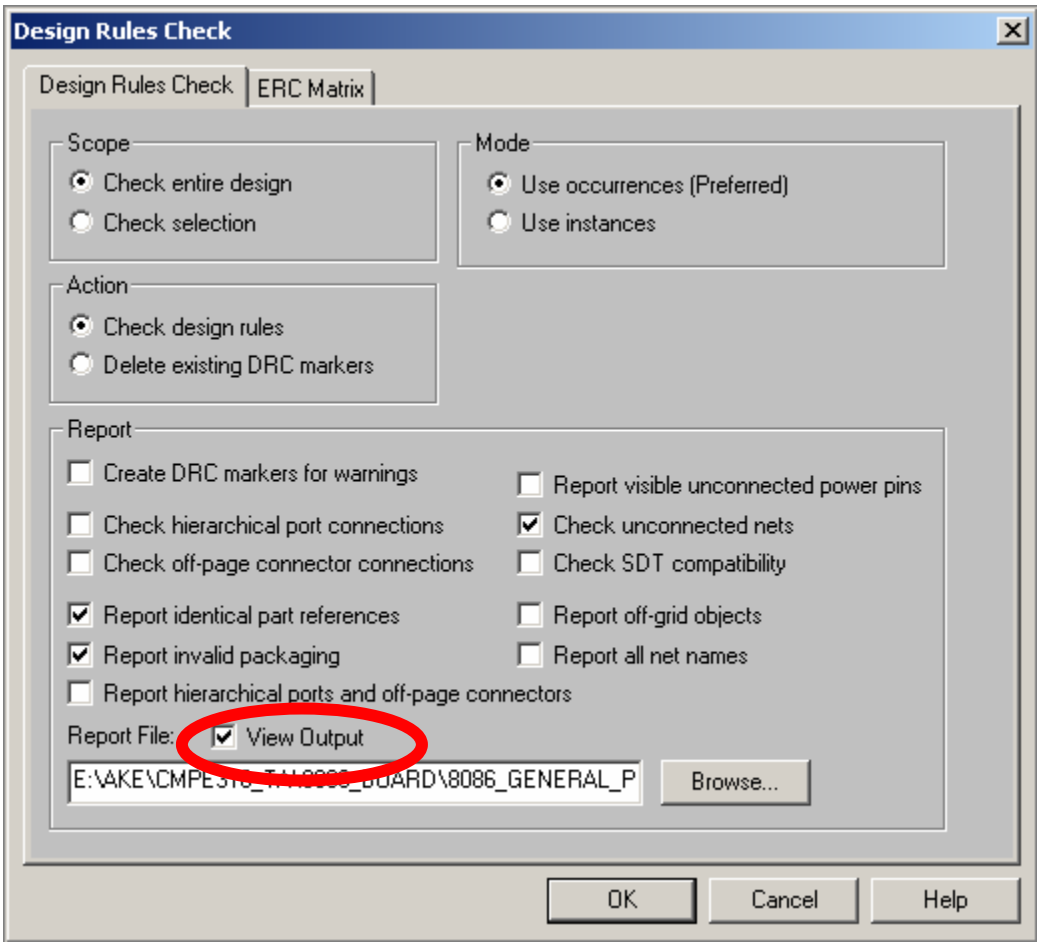

Figure 12: Design Rules Check

Creating Netlist

To import your design into PCB design tool, you will need to generate a netlist of your design. First, click on the schematic folder on the project window and go to **Tool → Create Netlist**. You will see the Create Netlist dialog box as shown in Figure 13. Click on "Layout" tab and then type the location and file name to be saved on Netlist File textbox, use "**.MNL**" extension for your output file. Click OK and you will get a **netlist that is compatible with Cadence Layout Plus**, a PCB design tool.

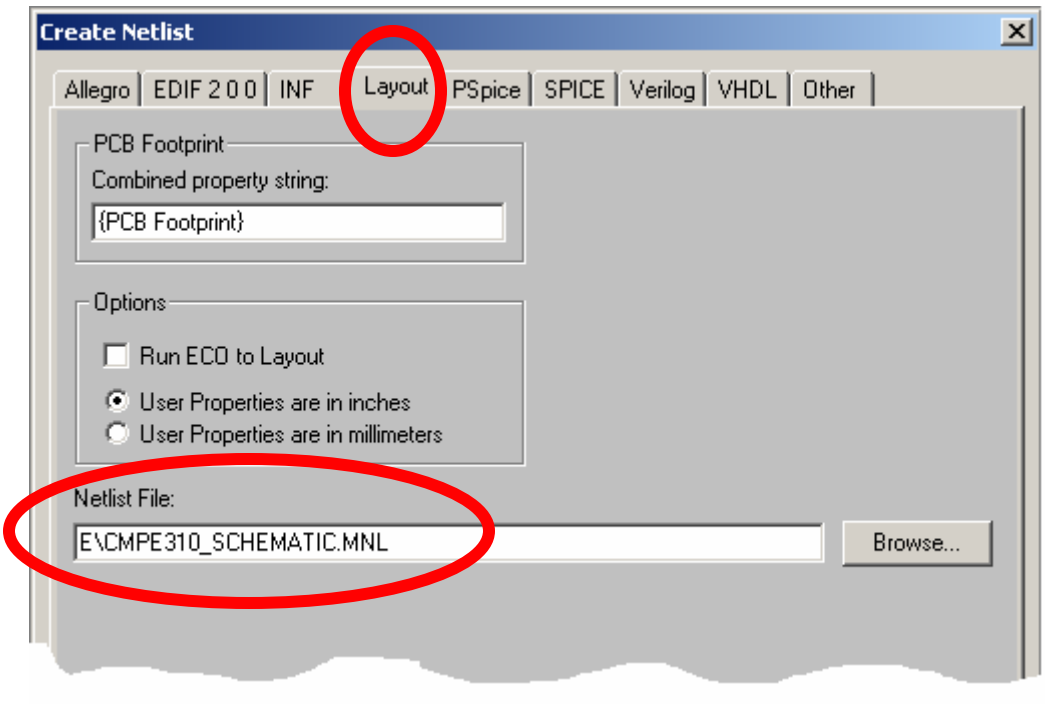

Figure 13: Create Netlist

More info:

- Important information about the parts of your design is embedded into a net list file and they will be used by PCB design tool. For example, part reference, part footprint and so on. It is easier to specify a footprint associated with a particular part before import the netlist into PCB tool. These footprints tell the PCB tool about the dimension, number of pins and package type of the part (ex. PDIP-20 is a Plastic Dual In-line Package with 20 pins) that are critical during place and route processes of PCB design.
- The **footprint library** is needed for specify a footprint for the part. You can use existing footprints on the local library for some package types. However, if you can't find a correct footprint for your part, you might need to make one by looking at the package drawing of the part and draw a new footprint using Layout Plus Library Manager.
- Again, we are so nice! that we include all footprints for all the parts you'll need for cmpe310 project in the library. So you do not worry about this issue.