CMSC 411—Homework 1

1. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c. For each processor, we are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rates should we have to get this time reduction?

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2. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0×10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D:

a. Which implementation is faster?

b. What is the global CPI for each implementation?

c. Find the clock cycles required in both cases.

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3. "MIPS"—"millions of instructions per second" (the actual instruction-counting measure, not the adjusted "VAX MIPS"-type number) is notoriously unreliable as a benchmarking measure. Give one reason why, and show how you could take advantage of this to write a benchmarking program that yields inflated MIPS measures.

Adapted slightly from questions courtesy Patterson, D., Hennessy, L.. *Computer Organization and Design: The Hardware/Software Interface, 5th Edition.* Morgan Kaufmann, 09/2013. VitalBook file.