Name:_____

Section	Points
I.	/26
II.	/30
III.	/50
TOTAL:	/106

Instructions:

1. This is a closed-book, closed-notes exam.
2. You have 120 minutes for the exam.
3. Calculators are not allowed.

I. Multiple Choice (2 points each)

For each question in this section, circle **1** answer. Choose the best answer.

1. A two's complement overflow *cannot* occur when

   (a) two positive numbers are added.
   (b) two negative numbers are added.
   (c) a positive number is added to a negative number.
   (d) a positive number is subtracted from a negative number.

2. In *unsigned* binary representation, an overflow is indicated when two numbers are added and

   (a) there is a carry out of the most-significant bit (MSB).
   (b) there is a carry into the MSB.
   (c) the carry into the MSB differs from the carry out of the MSB.
   (d) the carry into the MSB equals the carry out of the MSB.

3. Suppose we use a floating-point representation with a sign bit, a 4-bit exponent in excess 7 notation and a 5-bit normalized fractional mantissa with no hidden bit. Then, the largest number that can be represented is

   (a) 31×2^3
   (b) 31×2^8
   (c) 31×2^{13}
   (d) 0.31×2^8

4. When the Intel Pentium CPU executes a CALL instruction

   (a) the `eip` register is saved in the stack.
   (b) the `eip`, `ebp` and `esp` registers are saved in the stack.
   (c) the `eax`, `ecx`, `edx` and `eip` registers are saved in the stack.
   (d) none of the registers are saved.

5. Consider the following Intel Pentium instruction

   ```
   mov     [ebx], dword 5
   ```

   The keyword "DWORD" is needed to

   (a) indicate that 5 is an immediate operand.
   (b) indicate that 5 is an indirect operand.
   (c) indicate that 5 is an address.
   (d) indicate that 5 is a 32-bit number.

6. What is the effect of the following instruction?

```
mov     ecx, [ebp + 8]
```

   (a) Add 8 to the contents of `ebp` and store the sum in `ecx`.

   (b) Add 8 to the contents of `ebp`, treat the sum as a memory address and store the contents at that address in `ecx`.

   (c) Add 8 to the contents of the memory location whose address is stored in `ebp` and store the sum in `ecx`.

   (d) Add the contents of `ebp` to the contents of memory address 8 and store the sum in `ecx`.

7. The instruction

```
cmp     eax, ebx
```

   (a) performs a signed subtraction of `ebx` from `eax` and sets the `eflags` register accordingly.

   (b) performs an unsigned subtraction of `ebx` from `eax` and sets the `eflags` register accordingly.

   (c) performs both a signed and an unsigned subtraction of `ebx` from `eax` and sets the `eflags` register accordingly.

   (d) performs a signed subtraction only when `eax` and `ebx` contain numbers in two's complement and sets the `eflags` registers accordingly.

8. Which of the following is *not* an advantage of the virtual memory system used by Linux on the Pentium CPU:

   (a) increases the apparent amount of memory available to applications.

   (b) reduces the average memory access time.

   (c) provides memory protection between applications.

   (d) provides memory protection between the operating system and applications.

9. Suppose that an assembly language program calls a C function `foo`. Then in the instruction

```
call    foo
```

   the address of `foo` is determined

   (a) during the first pass of the two-pass assembler.

   (b) during the second pass of the two-pass assembler.

   (c) when the C source code for `foo` is compiled.

   (d) during the linking phase of the linking loader.

10. The PDP-8 instructions accessed operands across the entire address space by using

    (a) index registers.
    (b) indirect addressing.
    (c) relative addressing.
    (d) none of the above.

11. The PDP-8 word size was

    (a) 8 bits.
    (b) 12 bits.
    (c) 16 bits.
    (d) 2 bytes.
    (e) variable.

12. A combinational logic circuit

    (a) implements a Boolean function.
    (b) has no memory.
    (c) can always be implemented with NAND gates only.
    (d) can always be implemented in a sum-of-products form.
    (e) all of the above.

13. Compared to a ripple-carry adder, a carry-lookahead adder

    (a) can be implemented with fewer gates.
    (b) can operate faster because it has fewer levels of logic.
    (c) has inputs applied sequentially rather than in parallel.
    (d) a and c are both true.
    (e) none of the above.

II. Short Answers (3 points each)

For each question in this section, *show all of your work.* Clearly indicate your final answer.

1. Give the binary representation of -67 in each of the following data representations

   (a) 8-bit one's complement

   (b) 8-bit two's complement

   (c) 8-bit excess 127

2. A floating point representation uses a sign bit, a 4-bit exponent in excess 7 notation, and a 5-bit fractional mantissa with no hidden bit. What number is represented by the binary sequence: 1 1101 10110

3. Convert 127_{10} in base 6.

4. Multiply the following 4 bit two's complement numbers: 1001×0110. What is the result in decimal?

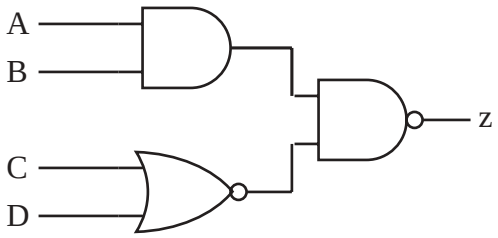
5. What is the difference between a software and a hardware interrupt?

6. Using any means you desire, simplify the following Boolean expressions:

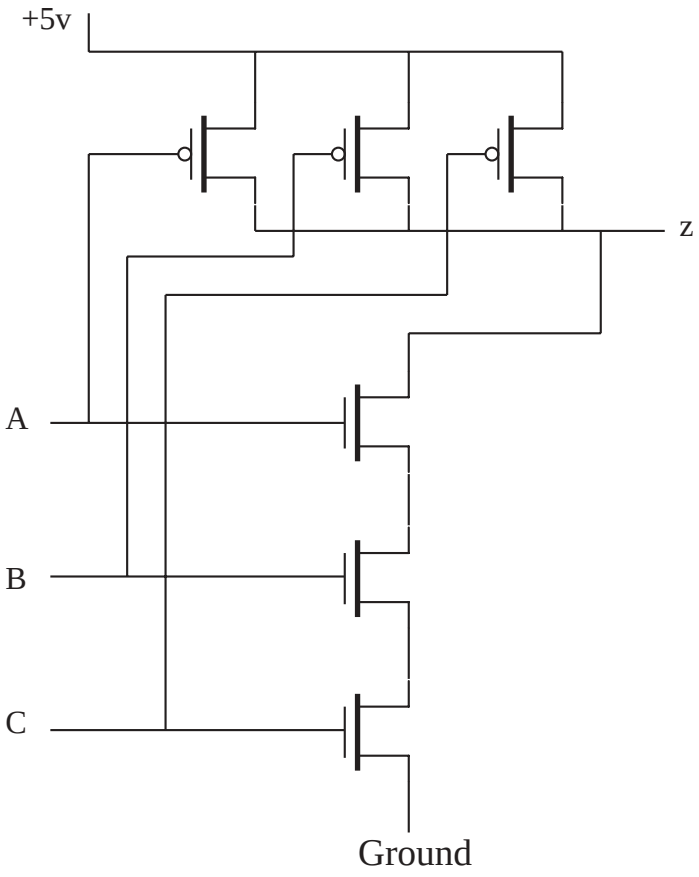
   (a) $A\,B + \overline{A}\,B\,C$

   (b) $A\,B + \overline{A}\,C + B\,C$

7. What logic function is realized by the circuit below? Note the bubbles.

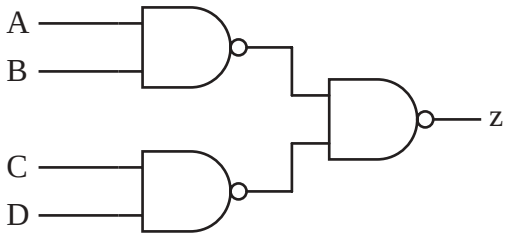


8. What logical operation is performed by the transistor circuit below?



9. Draw the circuit diagram of a D latch with an enable input. Label the inputs and outputs.

10. Use deMorgan's law to draw an equivalent logic circuit to the one below, but which uses only AND and OR gates.



III. Problems (10 points each)

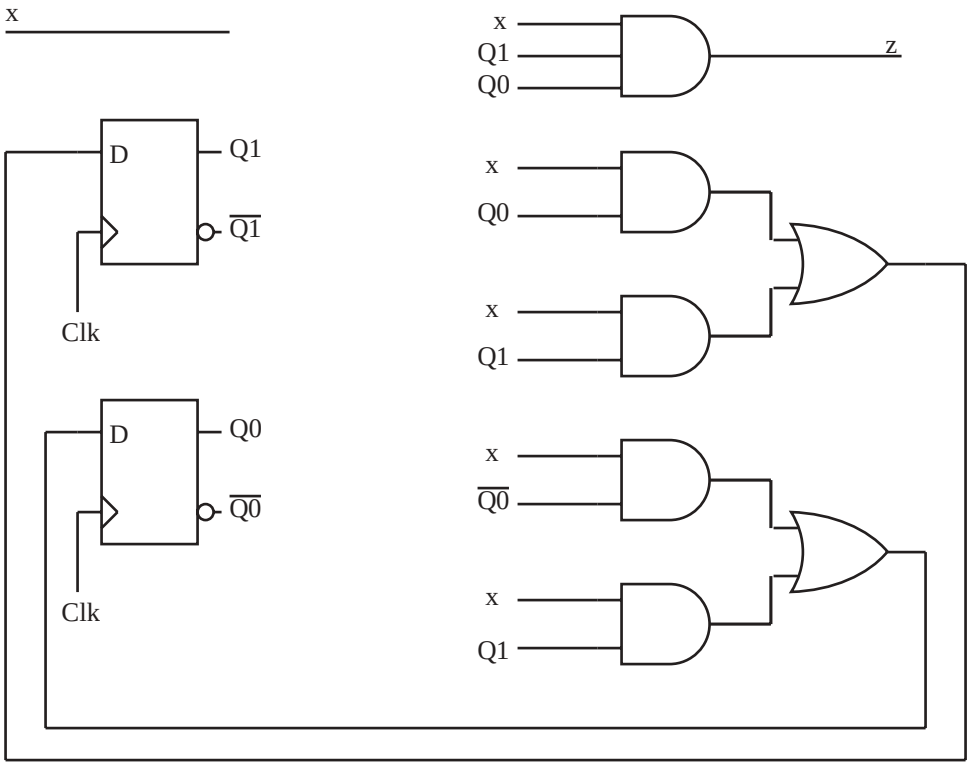
1. Suppose that the `esi` register contains the address of the first character of a string and the `ecx` register contains the number of characters in the string. Write an assembly language program for the Intel Pentium CPU that finds the first occurrence of the character `'a'` in the string and stores its address in the `eax` register. If the string contains no occurrence of the letter `'a'`, the `eax` register must be zero.

2. Give a minimized sum-of-products logic circuit for the Boolean function

$$F(A, B, C) = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C} + \overline{A}\,B\,C + A\,B\,\overline{C} + A\,B\,C$$

3. Design a combinational logic circuit which will compare 2 two-bit unsigned integers x and y, $x = (x_1, x_0)$ and $y = (y_1, y_0)$, and produces a Boolean output z which is a one when $x \geq y$ and zero otherwise. Show its implementation in a reduced sum-of-products form.

4. Given the sequential circuit below, fill in the rest of the state transition table giving the next state and output as functions of the present state and input.



		x = 0	x = 1
Q1Q0	00	00/0	
	01		
	10		
	11		

The entries of the table are the next states $Q1'$ $Q2'$ followed by the output z.

5. A sequential circuit is to be designed to recognize the occurrence of the input pattern 1011, i.e. its output is to be a one when the most recent inputs have been 1011, and zero otherwise. Define an appropriate set of states and draw the state transition diagram for such a machine. Label the transitions with the input and associated output values.

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