Spring 2009: CMPE 640 Project Specification

Project Specification: Cache Design
(Please refer to the webpage for any changes to this specification over the next couple of weeks).

Assigned: Apr 10th
Due: Last Day of Class

Description:
Design a virtually-indexed physically-tagged cache. Following are the specification of the cache, the TLB and the processor/memory interface

■ Cache
  ❑ 1KB Direct Mapped
  ❑ 32-bit words, cache is word addressed
  ❑ 8 word blocks
  ❑ 32 blocks
  ❑ Write-through with no write-allocate
  ❑ 1 clock cycle read hit operation
  ❑ 2 clock cycle write hit operation
  ❑ Variable number of clock cycles for read miss operation, determined by the speed of the installed memory. A synchronous handshaking signal will be provided by the memory when the data is ready to be transferred. One word will be transferred per clock cycle after the activation of this signal.

■ Processor/Memory Interface
  ❑ 20-bit processor address bus
  ❑ 32-bit processor data bus
  ❑ 20-bit memory address bus
  ❑ 32-bit memory data bus
  ❑ Handshaking signals as required (e.g. TLB miss, cache miss, data ready, read/write). You can pick your own handshaking signals, but make sure you justify why you need them in your design. An example set will be discussed during the discussion session.

■ TLB/Paging System
  ❑ 4KB Pages
  ❑ 16 TLB locations
  ❑ First-in First-out replacement policy
  ❑ Should work for different amounts of installed memory. The physical address size will be provided as a parameter that can be stored in a register in your design.

The TLB has to be designed using CAM and SRAM cells and the cache using SRAM cells. Refer to Chapter 12 in the textbook. Also read [1] that provides details of various design techniques and proposes decoder and other architectures. For your decoder design and reset logic, you can use a technique similar to the one described in this document. Due to time constraints you are not required to design a sense amplifier for the SRAMs. Also as we haven’t discussed other logic styles in details most of the circuits should be designed using static CMOS.
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Generic Block Diagram

Grading, Report Requirements and Deadlines

The deadline for the project is the last day of classes May 12th. A detailed report describing your design, including detailed block diagrams for each stage, schematics, code and simulation results is required. We will discuss the submission requirements closer to the deadline.

Grading:

Working VHDL code: A VHDL structural description for the entire design along with testbenches and simulation results. You can model the TLB and the SRAMs using a behavioral description, everything else should have a structural description. (20 points)

TLB: A schematic and layout for the TLB, associated logic and results from post-layout simulations with detailed extracted parasitics (30 points)

Cache Block: A schematic and layout for the cache block, associated logic and results from post-layout simulations with detailed extracted parasitics (30 points)

Final Layout and Integration: The layout of the entire design and verification results (20 points)

10 extra points will be awarded competitively based on the compactness of the layout and the maximum operating frequency as determined from simulation results. You are responsible to identify the test cases required to determine the maximum operating speed for your circuit and
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provide simulation results and justification for the same in your report to be eligible for extra credit.

References