Ratioed Logic

One method to reduce the circuit complexity of static CMOS.

Here, the logic function is built in the PDN and used in combination with a simple load device.

Let's assume the load can be represented as linearized resistors.

When the PDN is on, the output voltage is determined by:

\[ V_{OL} = \frac{R_{PDN}}{R_L + R_{PDN}} V_{DD} \]
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This logic style is called ratioed because care must be taken in scaling the impedances properly.

Note that full complementary CMOS is ratioless, since the output signals do not depend on the size of the transistors.

In order to keep the noise margins high, \( R_L \gg R_{PDN} \).

However, \( R_L \) must be able to provide as much current as possible to minimize delay.

\[
t_{PLH} = 0.69 R_L C_L
\]
\[
t_{PHL} = 0.69 (R_L \parallel R_{PDN}) C_L
\]

These are conflicting requirements:

- \( R_L \) large: Noise margins.
- \( R_L \) small: performance and power dissipation.
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This has resulted in a wide variety of possible load configurations.

- Simple resistor
  - Available charge current as a function of the output voltage is linear:
    \[
    I_L = \frac{V_{DD} - V_{out}}{R_L}
    \]
  - Disadv: Charge current drops rapidly once \( V_{out} \) starts to rise.
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- Current source

  *Ideal* in the sense that the available current is independent of the output voltage. It is easy to prove that $t_{pLH}$ is reduced by 25% over the resistor load.

- Depletion load

  The depletion load gate shown previously emerged as the *most popular* gate in the NMOS era (up until the early 80s).

  The load is an NMOS depletion mode transistor (*negative threshold device*) with the gate connected to the output (source).

  Note that the device is on when $V_{GS} = 0$.

  The load acts as a **current source** (first-order), given by its saturation equation:

  $$I_L = \frac{k_{n,\text{load}}}{2} (|V_Tn|)^2$$
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- Depletion load (cont.)
  The load line *deviates* from the ideal current source for two reasons:
  
  (a) The *channel length modulation* factor modulates current in saturation mode.
  
  (b) The source of the load transistor is connected to the output of the inverter.

  The **body effect** causes the threshold of the load transistor to vary as a function of $V_{out}$.

  The body effect reduces $|V_{Tn}|$ and the available current for increasing values of $V_{out}$.

  Nevertheless, the depletion load out-performs the resistive load and requires less area!
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Pseudo-NMOS

A grounded PMOS device presents an even better load.

It is better than depletion NMOS because there is no body effect (its $V_{SB}$ is constant and equal to 0).

Also, the PMOS device is driven by a $V_{GS} = -V_{DD}$, resulting in a higher load-current level than a similarly sized depletion-NMOS device.

\[
I_L = \frac{k_p}{2}(V_{DD} - |V_{Tp}|)^2
\]

(ignoring channel length modulation)

The $V_{OH} (=V_{DD})$ from the dc transfer characteristic is the same as that for the full complementary device.

$V_{OL}$ differs from GND, however.
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- Pseudo-NMOS (cont)
  
  $V_{OL}$ can be obtained by equating the currents through the driver and load devices for $V_{in} = V_{DD}$.

  Here, the NMOS driver resides in linear mode while the PMOS load is in saturation:

  $k_n \left( (V_{DD} - V_{Tn})V_{OL} - \frac{V_{OL}^2}{2} \right) = \frac{k_p}{2} (V_{DD} - |V_{Tp}|)^2$

  Assuming $V_{Tn} = |V_{Tp}|$, solving for $V_{OL}$ yields:

  $V_{OL} = (V_{DD} - V_T) \left( 1 - \sqrt{1 - \frac{k_p}{k_n}} \right)$

  For example, if $k_p = k_n$, $V_{OL} = V_{DD} - V_T$, which is clearly unacceptable.

  For $r = k_p/k_n = 1/4$, $V_{OL} = (5 - 0.8) \cdot 0.134 \approx 0.56V$. 
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- Pseudo-NMOS (cont)

  Similarly, $V_M$ can be computed by setting $V_{in} = V_{out}$ and solving the current equations.

  This assumes the NMOS and PMOS are in saturation and linear, respectively.

  $$V_M = V_T + (V_{DD} - V_T) \sqrt{\frac{k_p}{k_n + k_p}}$$

Design challenges:
- This clearly indicates that $V_M$ is not located in the middle of the voltage swing (e.g. if they are equal, the square root yields 0.707).
- The rise and fall times are asymmetrical.
- This gate consumes static power when the output is low.

$$P_{av} = V_{DD}I_{low} = \frac{k_p}{2}V_{DD}(V_{DD} - V_T)^2$$
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- Pseudo-NMOS (cont)

Let's assume the load can be approximated as a *current source* for the entire operation region.

\[ \text{IL} \quad \text{Out} \]
\[ \text{RPDN} \]
\[ \text{In} \]

Trade-offs:

- To reduce static power, \( \text{IL} \) **should be low**.
- To obtain a reasonable \( \text{NM}_L \), \( V_{OL} = \text{IL} \times \text{RPDN} \) **should be low**.
- To reduce \( t_{PLH} \approx (C_L V_{DD})/(2\text{IL}) \), \( \text{IL} \) **should be high**.
- To reduce \( t_{PHL} \approx 0.69 \times \text{RPDN} C_L \), \( \text{RPDN} \) should be kept **small**.
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- Pseudo-NMOS (cont)

  The \( r = \frac{(W/L)_n}{(W/L)_p} \) in the expression for \( V_{OL} \) defines \( NM_L \).

  For example, to obtain a \( V_{OL} \) of 0.2V (1.2 um tech., \( V_{DD}=5V \)) requires a ratio of \( r=3 \). This also guarantees the 4th condition.

  However, 1 and 3 are contradictory: realizing a faster gate (\( t_{pLH} \)) means more static power consumption and reduced noise margin.

Pseudo-NMOS attractive for complex gates with large fan-in.

As mentioned, only N+1 transistors, smaller area and smaller parasitics.

Smaller downstream load capacitance.

However, static power consumption makes it impossible to use in large circuits (except in address decoders when majority of outputs are high).

A minimum sized gate consumes 1mW!
Even better loads

Consider the following modification to the pseudo-NMOS NOR.

Here, it is known that the inputs switch only during certain time periods. For example, an address decoder which should only switch when the address changes.

In stand-by mode, low power consumption and large noise margins.

For address change, high power fast \( t_{PLH} \) transition.
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Even better loads (cont)

It's possible to **completely eliminate** static current:

Differential Cascade Voltage Switch Logic (DCVSL).

PDN₁ and PDN₂ are complementary.

Assume PDN₁ conducts, input to M₂ is turned on, pulling up \( \overline{\text{Out}} \).

This in turn, shuts off M₁.

*Speed advantage* of pseudo-NMOS (reduced output parasitics) with *no static power consumption*, but occupies **extra area**.
**Ratioed Logic**

- Even better loads (cont)

However, transistors can be shared between PDN₁ and PDN₂.

This gate has been used to implement fast error-correcting logic in memories.

Plus, the availability of complementary signals eliminate extra inverter stages.