**Dynamic Behavior**

The transient behavior of a *pn-junction* was dominated by:
- The movement of *excess minority carrier charge* in the neutral zones.
- The movement of *space charge* in the depletion region.

MOSFETs are *majority carrier* devices.

Their dynamic behavior is determined solely by the time to:
- Charge and discharge the capacitances between the device ports.
- Charge and discharge of the interconnecting lines.

These capacitances originate from three sources:
- The basic MOS structure.
- The channel charge.
- The depletion regions of the reverse-biased pn-junctions of drain and source.

Aside from the MOS structure capacitances, all capacitors are *nonlinear* and vary with the *applied voltage*. 

MOS Structure Capacitances:

The gate of a MOS transistor is isolated from the channel by the gate oxide where:

\[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]

For the I-V equations, it is useful to have \( C_{ox} \) as \textbf{large} as possible, by keeping the oxide very thin.

This capacitance is called gate capacitance and is given by:

\[ C_g = C_{ox} WL \]

This gate capacitance can be decomposed into several parts:
- One part contributes to the channel charge.
- A second part is due to the topological structure of the transistor.

Let's consider the latter first.
Dynamic Behavior

MOS Structure Capacitances, Overlap:

Lateral diffusion: source and drain diffusion extend under the oxide by an amount $x_d$. The effective channel length ($L_{eff}$) is less than the drawn length $L$ by $2*x_d$.

This also gives rise to a linear, fixed capacitance called overlap capacitance.

$$C_{gsO} = C_{gdO} = C_{ox}x_dW = C_OW$$

Since $x_d$ is technology dependent, it is usually combined with $C_{ox}$. 

$$\text{poly}$$

source $n^+$

$W$

drain $n^+$

$\text{Poly}$

$n^+$

$L_{eff}$

$C_{gsO} = C_{gdO} = C_{ox}x_dW = C_OW$
Dynamic Behavior

Channel Charge

The gate-to-channel capacitance is composed of three components, $C_{gs}$, $C_{gd}$ and $C_{gb}$. Each of these is non-linear and dependent on the region of operation.

Estimates or average values are often used:
- Triode: $C_{gb} \approx 0$ since the inversion region shields the bulk electrode from the gate.
- Saturation: $C_{gb}$ and $C_{gd}$ are $\approx 0$ since the channel is pinched off.

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>$C_{gb}$</th>
<th>$C_{gs}$</th>
<th>$C_{gd}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$C_{ox}\cdot W_{eff}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Triode</td>
<td>0</td>
<td>$C_{ox}\cdot W_{eff}/2$</td>
<td>$C_{ox}\cdot W_{eff}/2$</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>$(2/3)C_{ox}\cdot W_{eff}$</td>
<td>0</td>
</tr>
</tbody>
</table>
**Dynamic Behavior**

**Junction or Diffusion Capacitances**

This component is caused by the reverse-biased source-bulk and drain-bulk *pn-junctions*.

We determined that this capacitance is **non-linear** and *decreases* as reverse-bias is *increased*.

---

![Diagram of MOS transistor](image)

- **Bottom-plate junction:**
  - Depletion region capacitance is:
  
  \[ C_{\text{bottom}} = C_j W L_S \]

  with a grading coefficient of \( m = 0.5 \) (for an abrupt junction)
Dynamic Behavior

MOS Structure Capacitances, Junction or Diffusion:

- Side-wall junction

  Formed by the source region with doping $N_D$ and the $p^+$ channel-stop implant with doping $N_A^+$. Since the channel-stop doping is usually higher than the substrate, this results in a higher unit capacitance:

  $$ C_{sw} = C'_{jsw} x_j (W + 2 \times L_S) $$

  with a grading coefficient of $m = 1/3$.

  Note that the channel side is not included in the calculation. $x_j$ is usually technology dependent and combined with $C'_{jsw}$ as $C_{jsw}$.

Total junction (small-signal) capacitance is:

$$ C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER $$

$$ C_{diff} = C_j L_S W + C_{jsw} (2L_S + W) $$

As we've done before, we linearize these and use average cap.
Dynamic Behavior

Capacitive Device Model

The previous model can be summarized as:

\[ G \]

\[ S \]

\[ C_{GS} \]

\[ C_{SB} \]

\[ C_{GB} \]

\[ C_{GD} \]

\[ C_{DB} \]

\[ D \]

\[ B \]

\[ C_{GS} = C_{gs} + C_{gsO} \]

\[ C_{GD} = C_{gd} + C_{gdO} \]

\[ C_{GB} = C_{gb} \]

\[ C_{SB} = C_{Sdiff} \]

\[ C_{DB} = C_{Ddiff} \]

The dynamic performance of digital circuits is directly proportional to these capacitances.
Dynamic Behavior

Example:

Given:

\[ t_{ox} = 6\, \text{nm} \quad \quad C_{O} = 3 \times 10^{-10} \, \text{F/m} \]
\[ L = 0.24\, \text{um} \quad \quad C_{j0} = 2 \times 10^{-3} \, \text{F/m}^2 \]
\[ W = 0.36\, \text{um} \quad \quad C_{jsw0} = 2.75 \times 10^{-10} \, \text{F/m} \]
\[ L_D = L_S = 0.625\, \text{um} \]

Determine the zero-bias value of all relevant capacitances.

Gate capacitance, \( C_{ox} \), per unit area is derived as:

\[
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.5 \times 10^{-2} \, \text{fF/um}}{6 \times 10^{-3} \, \text{um}} = 5.8 \, \text{fF/um}^2
\]

Total gate capacitance \( C_g \) is:

\[
C_g = WLC_{ox} = 0.36\, \text{um} \times 0.24\, \text{um} \times 5.8 \, \text{fF/um}^2 = 0.5\, \text{fF}
\]

Overlap capacitance is:

\[
C_{GSO} = C_{GDO} = WC_O = 0.108\, \text{fF}
\]

Total gate capacitance is:

\[
C_{g_{tot}} = C_g + 2 \times C_{GSO} = 0.716\, \text{fF}
\]
**Dynamic Behavior**

Example (cont):

Diffusion capacitance is the sum of bottom:

\[
C_{j0L_DW} = 2 fF/\mu m^2 \times 0.625 \mu m \times 0.36 \mu m = 0.45 fF
\]

Plus side-wall (under zero-bias):

\[
C_{jsw0}(2L_D + W) = 2.75 \times 10^D \times (2 \times 0.625 \mu m + 0.36 \mu m) = 0.44 fF
\]

In this example, diffusion capacitance dominates gate capacitance (0.89 fF vs. 0.716 fF).

Note that this is the worst case condition. Increasing reverse bias reduces diffusion capacitance (by about 50%).

Also note that side-wall dominates diffusion. Advanced processes use SiO₂ to isolate devices (trench isolation) instead of \(N_A^+\) implant.

Usually, diffusion is at most equal to gate, very often it is smaller.
Source-Drain Resistance

Scaling causes junctions to be *shallower* and contact openings to be *smaller*. This increases the parasitic resistance in series with the source and drain.

![Diagram of MOS Transistor with source and drain](image)

This resistance can be expressed as:

\[ R_{S,D} = \frac{L_{S,D}}{W} R_\square + R_C \]

- \( R_C \) = Contact Resistance
- \( R_\square \) = Sheet resistance (2Ω ÷ 100Ω)
- \( L_{S,D} \) = length of source/drain region.

The series resistance degrades performance by decreasing drain current.

Silicidation used -- low-resistivity material such as *titanium* or *tungsten*. 
Secondary Effects

Long-channel devices

One-dimensional model discussed thus far.
Assumed:
- All current flows on the surface of the silicon.
- Electric fields are oriented along that plane.

Appropriate for manual analysis.

Short-channel device

Ideal model does not hold well when device dimensions reach sub-micron range.
- The length of the channel becomes comparable to other device parameters such as the depth of the drain and source junctions.
- Two-dimensional model is needed.

Computer simulation required.
**Secondary Effects**

**Threshold variations**

Ideal model assumed *threshold voltage* was only a function of technology parameters and applied body bias, $V_{SB}$.

With smaller dimensions, the $V_{T0}$ becomes a function of $L$, $W$ and $V_{DS}$.

For example, the expression for $V_{T0}$ assumed that all depletion charge beneath the gate originates from the MOS field effects.

We ignored the source and reverse-biased drain depletion regions. These depletion regions extend under the gate, which in turn reduces the threshold voltage necessary to cause strong inversion.

Threshold as a function of length (for low $V_{DS}$)

Drain-induced barrier lowering for small $L$. 

---

**Diagram:**

- Long-channel threshold
- Short-channel threshold
- Drain-induced barrier lowering for small $L$. 

---

**Graph:**

- $V_T$ vs. $L$
- $V_T$ vs. $V_{DS}$
**Secondary Effects**

**Threshold variations**

Also, threshold decreases with increasing $V_{DS}$.

This effect is called *drain-induced barrier lowering (DIBL)*.

For high values of $V_{DS}$, the source and drain depletion regions can short together (punch-through).

**DIBL** is a more serious issue than the variation in $V_{T0}$ as a function of length (since most transistors are minimum length transistors).

Particularly for DRAMs.

Leakage current of a cell (e.g. subthreshold current of the access transistor) is a function of voltage on the data line.

![Diagram of a DRAM cell showing the connections between the word-line, data line, $C_x$, and $C_{bit}$, with a shared capacitor highlighted.](image)
Secondary Effects

Threshold variations

Threshold drift also occurs for short-channel devices over time as a result of \textit{hot-carrier effects}.

In the past, \textit{constant voltage scaling} was used which increased the electric field strength and velocity of the electrons.

The electrons can leave the silicon and tunnel into the gate oxide, given enough energy.

Trapped electrons in the oxide \textit{increase} the threshold of NMOS devices and \textit{decrease} the threshold of PMOS devices.

Field strengths of $10^4$V/cm are easily reached in submicron devices.

This problem causes \textit{long-term reliability problems}. 
Secondary Effects

Variations in the I-V characteristics:

The current-voltage relations deviate significantly from the ideal expressions. The ideal expressions are:

\[ I_D = \frac{1}{2} \mu_n \left( \frac{\varepsilon_{ox}}{t_{ox}} \right) \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad \text{(Saturation)} \]

\[ I_D = \mu_n \left( \frac{\varepsilon_{ox}}{t_{ox}} \right) \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} \frac{V_{DS}^2}{2} \right] \quad \text{(Linear)} \]

The most important reasons for this difference are:

- **Velocity saturation effects**
- **Mobility degradation effects**
**Secondary Effects**

**Velocity Saturation**

We modeled carrier mobility, $\mu_n$, as a constant.

We stated carrier velocity is proportional to the electric field, independent of its value.

This holds up to a critical value of electric field, $E_c$, after which the velocity of the carriers tends to saturate:

Electrons in p-type silicon:

$$E_c = 1.5 \frac{V}{\mu m}$$

$$v_{sat} = 10^7 \frac{cm}{sec}$$

Therefore, only about 2 volts are needed for NMOS devices with a channel length of 0.25mm.

Holes in n-type silicon:

$$E_c > 10 \frac{V}{\mu m}$$

$$v_{sat} = 10^7 \frac{cm}{sec} \text{ (same)}$$
Secondary Effects

Velocity Saturation

Revised linear equation:

\[ I_D = \frac{\mu_n C_{ox}}{1 + \left(\frac{V_{DS}}{\xi c L}\right)} \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \]

\[ I_D = (\mu_n C_{ox}) \left(\frac{W}{L}\right) \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \kappa(V_{DS}) \]

with \[ \kappa(V) = \frac{1}{1 + \left(\frac{V}{\xi c L}\right)} \]

For long-channel devices (L is large) or small values of \( V_{DS} \), \( \kappa \) approaches 1, and the equation simplifies to the traditional equation.

For short channel devices, \( \kappa \) is less than 1 and current is reduced.
Secondary Effects

Velocity Saturation

Revised saturation equation:

\[ I_{DSAT} = v_{sat}C_{ox}W(V_{GS} - V_T - V_{DSAT}) \]

\[ I_D = \kappa(V_{DSAT})\mu_nC_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right] \]

with \( V_{DSAT} = \kappa(V_{GS} - V_T)(V_{GS} - V_T) \)

Further increases in \( V_{DS} \) does NOT yield more current and the transistor current saturates at \( I_{DSAT} \).

For \( V_{DSAT} < V_{GS} - V_T \) (for short channel devices), the device enters saturation before \( V_{DS} \) reaches \( V_{GS} - V_T \).

Saturation region is extended.
Secondary Effects

Velocity Saturation

This yields a \textit{linear} relationship between the saturation current and the gate-source voltage.

Long-channel devices

\[
V_{DS} = V_{GS} - V_T
\]

\begin{align*}
I_{DS} (mA) & \quad V_{GS} = 1V \\
& \quad V_{GS} = 2V \\
& \quad V_{GS} = 3V \\
& \quad V_{GS} = 4V \\
& \quad V_{GS} = 5V \\
\end{align*}

Short-channel devices

\[
V_{DS} = V_{GS} - V_T
\]

\begin{align*}
I_{DS} (mA) & \quad V_{GS} = 1V \\
& \quad V_{GS} = 2V \\
& \quad V_{GS} = 3V \\
& \quad V_{GS} = 4V \\
& \quad V_{GS} = 5V \\
\end{align*}

\[
W = 100 \mu m \\
L = 20 \mu m
\]

\[
W = 4.6 \mu m \\
L = 1.2 \mu m
\]

Extended saturation region (to be discussed).

Linear relationship with \( V_{GS} \)

However, reducing the operating voltage does \textbf{not} have such a significant effect in submicron devices as it would for long-channel devices.
Secondary Effects

Mobility Degradation

*Mobility degradation* is a second effect of reducing channel-length. This reduces transistor current even at "normal" electric field levels.

The reduction in the *electron mobility* is caused by the *vertical* component of the electric field (which was ignored before).

![Graph showing Mobility Degradation]

- $\mu_n$ is the electron mobility.
- $E_t$ is the transversal electrical field.
- $\mu_n0$ is the initial mobility.
- The graph shows a decrease in mobility as $E_t$ increases.
Secondary Effects

Subthreshold Conduction

The transistor is partially conducting for voltages below the threshold voltage. The region is referred to as *weak-inversion*.

V_{DS} is held constant at 5V.

Right logarithmic plot shows current decays in an exponential fashion.
Secondary Effects

Subthreshold Conduction

In the absence of a conducting channel, the \( n^+ \) (source) - p (bulk) - \( n^+ \) (drain) terminals actually form a \textit{parasitic bipolar transistor}.

The rate of decrease of current is described by:

\[
I_D = I_S e^{V_{GS}/nkT/q} \left(1 - e^{-V_{DS}/kT/q}\right) \left(1 + \lambda V_{DS}\right)
\]

where \( I_S \) and \( n \) are empirical parameters \((n \sim 1.5)\)

Ideally, \( I_D \) should fall to zero very quickly after \( V_{GS} \) falls below \( V_T \).

The \textit{inverse} rate of decline of the current w.r.t. \( V_{GS} \) below \( V_T \) is a quality measure of a device, and can be quantified by the **slope factor** \( S \).

\[
S = n \left(\frac{kT}{q}\right) \ln(10) \quad \text{mV/decade}
\]

\( S \) measures by how much \( V_{GS} \) has to be reduced for the drain current to drop by a factor of 10.
Secondary Effects

Subthreshold Conduction

For an ideal transistor, with the sharpest possible roll off, \( n = 1 \) and \( \frac{kT}{q}\ln(10) \) evaluates to 60 mV/decade at room temperature.

Therefore, subthreshold current drops by a factor of 10 for a reduction in \( V_{GS} \) of 60 mV.

Unfortunately, \( n \) is greater than 1 for actual devices and current falls at a reduced rate (90 mV/decade for \( n = 1.5 \)).

The current roll-off is further decreased by a rise in operating temperature (most chips operate at a temperature considerably above room temp).

Minimizing these leakages is particularly important in dynamic circuits, which store logic values as charge on a capacitor.

The value of \( n \) is affected by different process technologies, e.g., SOI.
SPICE Models

The complexity of the behavior of the short-channel MOS transistor has resulted in a variety of models of different accuracy and computing efficiency.

The LEVEL parameter in the model statement selects the model:

- **LEVEL 1:**
  - Implements the *Shichman-Hodges* model, which is based on the square law long-channel expressions.
  - Best used to verify a manual analysis.

- **LEVEL 2:**
  - Geometry-based model, which uses *detailed device physics* to define its equations.
  - It handles effects such as *velocity saturation, mobility degradation* and *DIBL* but is too complex and inaccurate to handle all 3D effects.
SPICE Models

- **LEVEL 3:**
  A semi-empirical model (depends on measured device data to define its parameters).
  Works well for channel lengths down to 1 mm.

- **LEVEL 4 (LEVEL 49):**
  Berkeley Short-Channel IGFET Model (BSIM).
  Provides an analytically simple model that is based on a small number of parameters extracted from experimental data.
  It is accurate as well as simple and is the most popular model.

- **LEVEL 5 - n:**
  There are many other models supplied by SPICE vendors and semiconductor manufacturers.

Some of the parameters on the following slides are redundant.
For example, **PHI** can be computed from process model parameters.
User-defined values always override those that can be computed.
### SPICE Parameters LEVELs 1-3

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE Model Index</td>
<td></td>
<td>LEVEL</td>
<td></td>
<td>1</td>
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<tr>
<td>Zero-Bias Threshold Voltage</td>
<td>V_{T0}</td>
<td>VTO</td>
<td>V</td>
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<tr>
<td>Process Transconductance</td>
<td>k'</td>
<td>KP</td>
<td>A/V^2</td>
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<td>Body-Bias Parameter</td>
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<td>GAMMA</td>
<td>V^0.5</td>
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<tr>
<td>Channel Modulation</td>
<td>λ</td>
<td>LAMBDA</td>
<td>1/V</td>
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</tr>
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<td>Oxide Thickness</td>
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<td>TOX</td>
<td>m</td>
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<td>Lateral Diffusion</td>
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<td>LD</td>
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<tr>
<td>Metallurgical Junction Depth</td>
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<td>XJ</td>
<td>m</td>
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<tr>
<td>Surface Inversion Potential</td>
<td>2\</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
\phi_F | PHI    | V     | 0.6    |
| Substrate Doping                        | N_A, N_D | NSUB  | cm^{-3} | 0 |
| Surface-State Density                   | Q_{ss}/q | NSS   | cm^{-3} | 0 |
| Fast Surface-State Density              | NFS    | Q_{ss}/q | cm^{-3} | 0 |
| Total Channel Charge Coef               | NEFF   | -         | -     | 1             |
| Type of Gate Material                   | TPG    | -         | -     | 1             |
| Surface Mobility                        | \mu_0 | U0        | cm^2/V-sec | 600 |
| Maximum Drift Velocity                  | \nu_{max} | VMAX | m/s | 0 |
| Mobility Critical Field                 | E_{crit} | UCRIT | V/cm | 1.0E4 |
| Critical Field Exponent in MD           |        | UEXP      | -     | 0             |
### SPICE Parameters LEVELs 1-3

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transverse Field Exponent (mobility)</td>
<td>$U_{TRA}$</td>
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<td>-</td>
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</tr>
<tr>
<td>Source Resistance</td>
<td>$R_S$</td>
<td>$RS$</td>
<td>$\Omega$</td>
<td>0</td>
</tr>
<tr>
<td>Drain Resistance</td>
<td>$R_D$</td>
<td>$RD$</td>
<td>$\Omega$</td>
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</tr>
<tr>
<td>Sheet Resistance (Source/Drain)</td>
<td>$R/sq$</td>
<td>$RSH$</td>
<td>$\Omega/sq$</td>
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<tr>
<td>Zero-Bias Bulk Junction Cap</td>
<td>$C_{j0}$</td>
<td>$CJ$</td>
<td>$F/m^2$</td>
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<tr>
<td>Bulk Junction Grading Coeff.</td>
<td>$m$</td>
<td>$MJ$</td>
<td>-</td>
<td>0.5</td>
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<tr>
<td>Zero-Bias Side-Wall Junction Cap</td>
<td>$C_{jsw0}$</td>
<td>$CJSW$</td>
<td>$F/m$</td>
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<td>Side-Wall Grading Coeff.</td>
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<td>$MJSW$</td>
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<tr>
<td>Gate-Bulk Overlap Cap.</td>
<td>$C_{gbO}$</td>
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<td>$F/m$</td>
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</tr>
<tr>
<td>Gate-Source Overlap Cap.</td>
<td>$C_{gsO}$</td>
<td>$CGSO$</td>
<td>$F/m$</td>
<td>0</td>
</tr>
<tr>
<td>Gate-Drain Overlap Cap.</td>
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<td>$CGDO$</td>
<td>$F/m$</td>
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<tr>
<td>Bulk Junction Leakage Current</td>
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<td>$A$</td>
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<tr>
<td>Bulk Junction Leakage Current Density</td>
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<td>Bulk Junction Potential</td>
<td>$\phi_0$</td>
<td>$PB$</td>
<td>$V$</td>
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</tr>
</tbody>
</table>
**SPICE Individual Transistor Parameters**

The following parameters are specified on the device line, not within the transistor.

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drawn Length</td>
<td>L</td>
<td>L</td>
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<tr>
<td>Effective Width</td>
<td>W</td>
<td>W</td>
<td>m</td>
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<tr>
<td>Source Area</td>
<td>AREA</td>
<td>AS</td>
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</tr>
<tr>
<td>Drain Area</td>
<td>AREA</td>
<td>AD</td>
<td>m²</td>
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<tr>
<td>Source Perimeter</td>
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<td>PS</td>
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<td>0</td>
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<tr>
<td>Drain Perimeter</td>
<td>PERIM</td>
<td>PD</td>
<td>m</td>
<td>0</td>
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<tr>
<td>Squares of Source Diffusion</td>
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</tr>
<tr>
<td>Squares of Drain Diffusion</td>
<td>NRD</td>
<td></td>
<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>

Note that zero is assumed for many of these if left unspecified!

NRS and NRD multiply the sheet resistance \( R_{SH} \) specified in the model to give the series source and drain resistance.

M1 2 1 0 0 **NMOS** \( W=1.8U \) \( L=1.2U \) \( NRS=0.333 \) \( NRD=0.333 \) 
+ \( AD=6.5P \) \( PD=9.0U \) \( AS=6.5P \) \( PS=9.0U \)

M2 2 1 5 5 **PMOS** \( W=5.4U \) \( L=1.2U \) \( NRS=0.111 \) \( NRD=0.111 \) 
+ \( AD=16.2P \) \( PD=11.4U \) \( AS=16.2P \) \( PS=11.4U \)