**Static Behavior**

An **nMOS** transistor cross-section:

\[ V_{GS} = 0, \ V_{DS} = 0 \]

Under zero bias, two back-to-back \textit{pn}-junctions create a very high resistive path between source and drain.

Applying a **positive bias** \(V_{GS}\) to the gate (w.r.t. the source), creates a depletion region under the gate (repells mobile holes).

The depletion region is similar to the one occurring in a \textit{pn}-junction.
**Static Behavior**

**Inversion**

\[ V_{GS} > 0, \quad V_{DS} = 0 \]

Depletion region expressions are similar to the diode expressions:

\[
W_d = \frac{2 \varepsilon_{si} \phi}{q N_A} \quad \text{Width}
\]

\[
Q_d = \sqrt{2 N_A \varepsilon_{si} \phi} \quad \text{Space charge}
\]

\[ \phi = \text{potential at the oxide-silicon boundary} \]
**Static Behavior**

**Inversion**

At a critical value of $V_{GS}$, the substrate **inverts** to *n-type* material.

This is called strong inversion and occurs at a voltage that is twice the *Fermi Potential*:

$$\phi_F = -0.3\, \text{V} \text{ for typical p-type silicon substrates.}$$

Further increases in $V_{GS}$ do **not** increase the depletion layer width.

The charge is offset with additional inversion-layer electrons (sourced from the heavily doped $n+$ source region).

The **conductivity** of the n-channel is modulated by $V_{GS}$.

Under strong inversion, the **charge** in the depletion region is fixed and equals:

$$Q_{B0} = \sqrt{2qN_A\varepsilon_{si}} \left| -2\phi_F \right|$$
Static Behavior

Inversion

A substrate bias voltage, $V_{SB}$, increases the surface potential needed to create strong inversion to:

$$| -2\phi_F + V_{SB} |$$

$V_{SB}$ is normally positive for n-channel devices. This changes the charge in the depletion region:

$$Q_B = \sqrt{2qN_A\varepsilon_{si}} | -2\phi_F + V_{SB} |$$

The value of $V_{GS}$ where strong inversion occurs is threshold voltage, $V_T$.

$V_T$ depends on several components, many are material constants:
- difference in work function between gate and substrate material.
- oxide thickness
- Fermi voltage
- charge associated with impurities trapped at oxide-channel interface
- concentration of implanted ions
**Static Behavior**

$V_T$ also depends on substrate voltage, $V_{SB}$.

Rather than depend on the complete analytical form (which often is not a good predictor of $V_T$), an empirical parameter is used, $V_{T0}$.

$V_{T0}$ is the threshold voltage with $V_{SB} = 0$.

$$V_T = V_{T0} + \gamma \left( \sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F} \right) \quad V_T \text{ is positive for nMOS and negative for pMOS}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \quad (\gamma \text{ is the body effect coefficient})$$

$\gamma$ expresses the impact of changes in $V_{SB}$.

A negative bias on the well or substrate causes $V_T$ to **increase**.

Given:

$$V_{T0} = 0.75\, V \quad \gamma = 0.54 \quad 2\phi_F = -0.64\, V \quad V_{SB} = 5\, V$$

$$V_T = 0.75 + 0.54 \left( \sqrt{-2(-0.6) + 5} - \sqrt{-2(-0.6)} \right) = 1.6\, V!$$
Static Behavior

Current-Voltage Relations

$V_{GS} > V_T, V_{DS} > 0$

- **Linear Region**

At a point $x$ along the channel, the voltage is $V(x)$.

The gate-to-channel voltage at that point equals $V_{GS} - V(x)$.
Static Behavior

Linear region

Assume that this voltage exceeds the threshold everywhere along the channel.

The induced channel charge per unit area at point $x$ is:

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T]$$

The gate capacitance per unit area, $C_{ox}$, is expressed as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\varepsilon_{ox} = 3.97 \times \varepsilon_0 = 3.5 \times 10^{-13} \text{ F/cm}$$

$t_{ox}$ is gate oxide thickness.

It is 10 nm or smaller in contemporary processes.

For $t_{ox} = 5$ nm, $C_{ox}$ is $7 \text{ fF/um}^2$. 
**Static Behavior**

**Linear region**

Current is given as the product of the *drift velocity* of the carriers and the available *charge*:

\[ I_D = -\nu_n(x)Q_i(x)W \]

\[ \nu_n = \text{drift velocity} \]

\[ W = \text{width of channel} \]

The *electron velocity*, \( \nu \), is related to the electric field through a parameter called the mobility (\( \mu \)):

\[ \nu_n = -\mu_n E(x) = \mu_n \frac{dV}{dx} \]

Combining the equations:

\[ I_D dx = \mu_n C_{ox} W(V_{GS} - V - V_T) dV \]
Static Behavior

Linear region

Integrating this equation over the length of the channel yields the current-voltage relationship of a nMOS transistor.

\[
I_D = k_n' \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

(1)

\[
k_n = k_n' \frac{W}{L}
\]

(gain factor)

\[
k_n' = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}
\]

(process transconductance parameter)

For typical n-channel devices with: \( t_{ox} = 20\text{nm} \)

\[k_n' = 80\mu A/V^2\]

For small values of \( V_{DS} \), the quadratic factor can be ignored and we observe a linear relationship between \( V_{DS} \) and \( I_D \).

NOTE: \( W \) and \( L \) are effective width and length, not the drawn values.
Static Behavior

Saturation

When $V_{DS}$ is further increased, the channel voltage all along the channel may cease to be larger than the threshold, e.g.,

$$V_{GS} - V(x) < V_T$$

At that point, the induced charge is zero and the channel disappears or is pinched off.

$V_{GS} > 0, V_{DS} > 0$
**Static Behavior**

**Current-Voltage Relation: Saturation**

The voltage difference over the *induced channel* remains fixed at $V_{GS} - V_T$ and the current remains constant (or saturates).

Replacing $V_{DS}$ with $V_{GS} - V_T$ in equation (1) (since this equation was derived over the channel) yields:

$$I_D = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_T)^2$$  \hspace{1cm} (2)

This equation is not entirely correct, since the channel length changes as a function of $V_{DS}$.

Current **increases** as channel length (L) **decreases**, according to equation (2).

A more accurate expression for current in saturation is:

$$I_D = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$\lambda$: empirical parameter called *channel-length modulation*
Static Behavior

Current-Voltage curves

I-V nMOS transistor curves for a device with dimensions:
- \( W = 100 \mu m \)
- \( L = 20 \mu m \)
in a 1.2\(\mu m\) process.
**Static Behavior**

**Current-Voltage Relation**

**Triode region**: The transistor behaves like a voltage-controlled resistor.

**Saturation region**: It behaves like a voltage-controlled current source (ignoring channel-length modulation effects).

Linear relationship for values:
\[ V_{GS} > V_T \]

Note: Analytical expressions of \( \lambda \) have proven inaccurate. Device experiments indicate that \( \lambda \) varies ~ 1/channel length.
**Static Behavior**

**Manual Analysis Model**

\[ V_{DS} > V_{GS} - V_T \]

\[ I_D = \frac{k_n' W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ V_{DS} < V_{GS} - V_T \]

\[ I_D = k_n' \frac{W}{L} \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right] \]

with

\[ V_T = V_{T0} + \chi \left( \sqrt{ -2 \phi_F + V_{SB} } - \sqrt{ -2 \phi_F } \right) \]