PRESENTATION ON MODELLING AND SIMULATIONS

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Modeling of VLSI semiconductor manufacturing processes

• The manufacture of complex integrated circuits demanded by present-day system designers requires the assembly of a large number of interacting process steps.

• Many of these process steps cannot be chosen without considering the effect of the other steps involved in the manufacturing process. A great deal of understanding of the basic physical principles must be employed before a successful manufacturing process can be defined.
One of key modelling process is fault modelling here we model the faults which might be present in the chip like stuck at fault, delay fault, transition fault.

Inadequate insight into the physics of processing and manufacturing can cause many failures at subsequent stages so its important to take into account in modelling as well.
Logical fault Modelling

• Permanent and randomly occurring can be broadly described as the two classes of logical faults.
• Permanent ones are usually due to manufacturing defects.
• Their modelling is more rigorous but their detection if done is applicable for a wide area as owing to their spread over presence. But it has been found that modelling of such faults e.g. spot defect is quite tough as their models tend to be very complex.
Stuck at faults

• Though most primitive algorithms like D-Algorithm and Podem which helped in generating models for these faults didn’t take multiple faults at once they gave good results.

• More evolves algorithms like FAN and others help in generating less test vectors and test more faults thus saving time and money.
CIRCUIT MODELLING

- A lot of research has gone into formulation of CMOS device models.
- For example, analog circuit analysis is still a research area. A new model which takes into account bulk doping concentration, fixed oxide charge and effective carrier mobility, its superiority is owing to its not depending on $V_t$ (threshold voltage) and rather on above characteristics. As $V_t$ is dependent on capacitance and Fermi potential leading to more computing and related dependencies.
CIRCUIT MODELLING

• This model helps in building an analog circuit simulator which gives predictive power and higher control over outputs owing to control over physical parameters described before.
Electromagnetic Modelling of VLSI Circuits

- The fast clock speed devices and high-density interconnections of the multi-chip modules (MCMs) have created problems such as multiple reflections, crosstalk, skin effect, dispersion, leakage, radiation, etc.
- The traditional CAD tools are based upon the quasi-static analysis (QSA), which is a low frequency approximation of the Maxwell equations.
- With sub-nanosecond rise time and tight physical dimensions, the QSA is not generally valid. This is because the electrical characteristics, presented by skin effect loss, dispersion and so on are not properly taken into account by the QSA. The full-wave analysis of the electromagnetic (EM) performance of the 3D packaging structures is definitely needed.
Recently, a new category of orthogonal mathematical systems, "orthogonal wavelets," has emerged. The major advantages of the wavelets representation are their multi-resolution analysis (MRA), vanishing moments, and localization properties, both in the spatial and spectral domain. The boundary integral equations of the modeling work usually result in full matrices.

This enables us to solve real world 3D packaging problems under full-wave regime. We can convert these theoretical results into useful CAD tools for modeling the EM behavior of complex 3D interconnects, and transfer the field solutions into circuit parameters.
FAULT SIMULATION

• The previous models basically worked on gate level description and took single stuck at line faults into account—there were some major problems because of this—some logic elements like switching transistors and load devices could not be taken as logic elements delay faults could not be accounted for. Delays are represented by lumped delay elements unsuitable in many cases and sometimes logical values are also constrained (i.e. may be only 0 and 1 are available).
SOME IMPROVEMENTS

• A few shortcomings of existing simulators in the context of VLSI design and testing are considered. A fault simulation approach based on CSA (connector-switch-attenuator) theory is defined which overcomes many of these deficiencies.

• The CSA circuit elements and logic values needed to model combinational circuits are described and applied to the analysis of various types of MOS circuits. A charge-storage element called a well is introduced to simulate sequential behavior.

• It is shown that many fault types, including stuck-line faults, short circuits, open circuits, and delay faults can be modeled in a uniform and efficient manner.
LOGIC SIMULATION

• Logic simulation is used extensively to verify the VLSI circuits before fabrication.
• As time for testing tends to be the bottleneck parallel processing and deductively working simulation has fast replaced the older approaches.
But parallel processing simulations face some problems they are broadly compartmentalized as circuit structure, timing granularity, target architecture and synchronization of algorithm.

This synchronization algorithm helps multiple processors work on the same simulation, thus enhancing time utilization

And better performance results.

But they still need more Research and development on them.
THANK YOU