Emerging Technologies
— A Critical Review

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12/05/05
CMOS device and beyond
Outline

- CMOS device challenges
- Electronic Nanotechnology Devices
- conclusion
Moore’s Law and “Red Brick Wall”

- Moore’s law has been based on silicon because it allows increment changes in size to produce integral improvement in performance.

- Approaching a “Red Brick Wall”, challenges/ opportunity for semiconductor R&D.
# ITRS Highlights Scaling Barriers

## Table 2a High Performance Logic Technology Requirements—2003 ITRS

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>TECHNOLOGY NODE (nm)</td>
<td>100</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MPU GATE LENGTH</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Gate Dielectric Equivalent Oxide Thickness (EOT) (nm) [1]</td>
<td>1.3</td>
<td>1.2</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
<td>0.6</td>
<td>0.50</td>
<td>0.45</td>
</tr>
<tr>
<td>Electrical Thickness Adjustment Factor (Gate Depletion and Quantum Effects) (nm) [2]</td>
<td>0.8</td>
<td>0.8</td>
<td>0.7</td>
<td>0.7</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>Electrical Equivalent Oxide Thickness in Inversion (nm) [4]</td>
<td>2.1</td>
<td>2.0</td>
<td>1.8</td>
<td>1.7</td>
<td>1.3</td>
<td>1.2</td>
<td>1.1</td>
<td>1.0</td>
<td>0.90</td>
<td>0.9</td>
</tr>
<tr>
<td>Vdd (V) [4]</td>
<td>1.2</td>
<td>1.2</td>
<td>1.1</td>
<td>1.1</td>
<td>1.1</td>
<td>1.0</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
</tr>
</tbody>
</table>
Present-Day CMOS Limitations

- Feature sizes nearing physical limits
- Lithography. Fabrication process reaches limits
- Power consumption – major concern
- Quantum effects must be accounted for
- Solution? Nanotechnology
Emerging Technology Sequence
CMOS performance trend

- To sustain the historical trend for CMOS technology after 2010 requires new semiconductor material and structure. Even early if current bulk-Si data do not improve significantly
New Material & Non-Classical structures for CMOS

- Conventional Bulk CMOS
- SOI (silicon-on-insulator) $\leq 1.2 \times$ bulk
- Strained Si/SiGe $\leq 1.6 \times$ bulk
- Double-Gate $\leq 1.8 \times$ bulk

17%/Year
Antoniadis-ADT-01
Replace CMOS: New Devices and Architecture

- Conventional Si-based CMOS devices will eventually encounter a fundamental performance limit as their sizes are scaled down.

- The International Technology Roadmap for Semiconductors (ITRS) identifies promising avenues of research for developing technologies to eventually replace CMOS.
## Emerging Research Devices and Technologies

*Table 65  Estimated Parameters for Emerging Research Devices and Technologies in the year 2016*

<table>
<thead>
<tr>
<th>Technology</th>
<th>$T_{min}$ sec</th>
<th>$T_{max}$ sec</th>
<th>$CD_{min}$ m</th>
<th>$CD_{max}$ m</th>
<th>Energy J/µop</th>
<th>Cost min $/gate</th>
<th>Cost max $/gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si CMOS</td>
<td>3E-11</td>
<td>1E-6</td>
<td>5E-9</td>
<td>5E-6</td>
<td>4E-18</td>
<td>1E-11</td>
<td>3E-3</td>
</tr>
<tr>
<td>RSFQ</td>
<td>1E-12</td>
<td>5E-11</td>
<td>3E-7</td>
<td>1E-6</td>
<td>2E-18</td>
<td>1E-3</td>
<td>1E-2</td>
</tr>
<tr>
<td>Molecular</td>
<td>1E-8</td>
<td>1E-3</td>
<td>1E-9</td>
<td>5E-9</td>
<td>1E-20</td>
<td>1E-12</td>
<td>1E-10</td>
</tr>
<tr>
<td>Plastic</td>
<td>1E-4</td>
<td>1E-3</td>
<td>1E-4</td>
<td>1E-3</td>
<td>4E-18</td>
<td>1E-7</td>
<td>1E-6</td>
</tr>
<tr>
<td>Optical (digital, all optical)</td>
<td>1E-16</td>
<td>1E-12</td>
<td>2E-7</td>
<td>2E-6</td>
<td>1E-12</td>
<td>1E-3</td>
<td>1E-2</td>
</tr>
<tr>
<td>NEMS (conservative)</td>
<td>1E-7</td>
<td>1E-3</td>
<td>1E-8</td>
<td>1E-7</td>
<td>1E-21</td>
<td>1E-8 $^{179}$</td>
<td>1E-5</td>
</tr>
<tr>
<td>Biologically Inspired</td>
<td>1E-13</td>
<td>1E-4</td>
<td>6E-6</td>
<td>5E-5</td>
<td>3E-25</td>
<td>5E-4</td>
<td>3E-1</td>
</tr>
<tr>
<td>Quantum</td>
<td>1E-16</td>
<td>1E-15</td>
<td>1E-8</td>
<td>1E-7</td>
<td>1E-21</td>
<td>1E3</td>
<td>1E5</td>
</tr>
</tbody>
</table>

*In this table $T$ stands for system cycle time (switching time), $CD$ stands for critical dimension (e.g., physical gate length), Energy is the intrinsic operational energy of one device, and Cost is defined as $/gate.*
Emerging Research Devices and Technologies
- Plastic Transistors

- Plastic Transistors – Thin film transistor (TFT) fabricate on plastic substrates.
- Plastic transistors have the potential to provide very low-cost, rugged large area electronics which have many potential applications.
- A process technology consisting just of printing operations on paper-based substrates would have an intrinsic cost structure similar to color inkjet printing today.
Emerging Research Devices and Technologies
- Optical

- Optical – Optical computing is based on using light transmission and interaction with solids for information processing. Its potential advantages related to the following
  - Optical beans do not interact with each other
  - Optical information processing functions can be performed in parallel
  - Ultimate high speed of signal propagation (speed of light)

- Some disadvantages of digital optical computing include:
  - The relatively large size of components
  - High-speed computation can be realized only at the expense of dissipated power
Emerging Research Devices and Technologies
- NEMS,

- NEMS – Nano-electro mechanical system, Mechanical digital signals are represented by displacement of solid rods.
- Low dissipation is possible because NEMS computation is logically reversible.
Emerging Research Devices
----Molecular Electronics

- **Molecular Electronics** - digital logic circuits designed using single molecules
- The significant scaling factor gained from molecular-scale devices
- Surmount critical dimension control problems of CMOS using self-assembling molecules
- **Molecular electronics** are the most futuristic devices among all discussed so far. They have a large potential, but there are huge obstacles that must be overcome.
- chemists, biologists, physicists and engineers develop an **interdisciplinary platform** for communicating the needs of the electronics industry in one direction and the possibilities of chemical synthesis and self-assembly concepts in the other.
“Top-down” and “bottom up” approach

- The present route to manufacturing of electronic device is called “top-down”.
- Nano-scientists are now developing a new approach based on self-assembly of atoms and molecules called ‘bottom up’.
- Expert opinion is that eventually the ‘top-down’ and ‘bottom-up’ approaches can both be combined into a single nanoelectronics manufacturing process. Such a hybrid method has the potential to lead to a more economical nano-manufacturing process.
Looking to the future

- Silicon based CMOS will be a major part of microelectronics for the foreseeable future.
- New nanoscale devices will encompass a broad range of fabrication methodologies and function modalities.
- Their near term applications will require nanoscale devices to be functionally and technologically compatible with silicon CMOS.
- In the longer term, charge-based nanoscale devices may be supplemented with one or more new information processing technologies using a quite new logic “state variable” or means of representing the bit.
THANK YOU