Test and Test Equipment

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CMPE 640
11/23/05
Testing

- Verifies that manufactured chip meets design specifications.
- Cannot test for every potential defect.
- Modeling defects as faults allows for passing and failing of chips.
- Ideal test would capture all defects and pass only chips that have no defects.
- Driving factor is cost.
Design for Testability (DFT)
What is it?

- Testing logic is added to a circuit in order to make testing of the circuit or chip less complex.
- The additional circuitry is used only when testing the circuit and thus issues of area and performance overhead, power consumption during testing, and efficiency of the test are important.
- BIST, BISR, SCAN
Design for Testability (DFT)
Why is it needed?

- Allows for testing of parts of the chip that would otherwise be untestable or difficult to test (i.e. sequential logic, hard to control logic).
- Makes the test generation and test application cost-effective.
- The better the DFT approach, the better the test coverage is, and thus more of the defects will be detected.
Manufacturing Test Cost

- There has been a large increase in the number of SOC (System-On-Chip) and SIP (System-In-Package) designs which use a mixture of digital, analog, RF, and mixed-signal. These chips have created a demand for an all-in-one test solution that will reduce the cost of tests for mixed technology designs.

- Problems:
  - Increasing test costs because these new chips break the traditional test equipment capability requirements.
  - Low-cost equipment solutions targeting DFT enabled devices do not scale into mixed technology space.

- Solution:
  - Increase test system configurability and flexibility, which would be a fundamental shift in test equipment architecture.
High Integration Designs

- Form factor and battery life of consumer products are driving chip integration.
- Large SOC designs will use reusable mixed technology design blocks, which will enable designers to put designs together with less effort.
- Problems:
  - Testing chips containing RF and audio circuits will be a major challenge if they also contain a large amount of noisy digital circuitry.
  - Analog DFT techniques must improve to simplify test interfacing and slow down test instrument capability demands.
  - Highly structured DFT approaches will be needed to test embedded cores. Each core will require unique attention when using DFT to enable test.
- Solutions:
  - Analog BIST has been suggested as a possible solution for testing of mixed-signal designs, but more research in this area is needed.
  - DFT must enable test reuse for reusable design cores to reduce test development time for highly complex designs.
Defects and Failure Mechanisms

- Process technology advancements are changing the kinds of physical defects which affect circuit functionality.
  - Examples:
    - Smaller vias are more susceptible to incomplete etch, which possibly leads to a greater number of resistive vias.
    - Change from subtractive Al to damascene Cu may cause metal opens.
    - Use of low-k dielectrics may increase the number of resistive bridges.
  - Changing circuit sensitivities are likely to make defects that did not previously affect the circuit capable of disrupting the entire circuit.
  - Examples:
    - Shorter clock cycles mean defects that cause 10’s or 100’s of picoseconds delays can cause system failures.
    - Increasing noise effects such as crosstalk and power/ground bounce decrease timing and noise margins making circuit more susceptible to delay defects.
  - Important to know about upcoming technology advancements so that tests, fault models, and diagnosis tools can be developed that will detect the defects of future circuits.
Reducing Cost of Testing

- Test development time and cost will be reduced further by DFT techniques, test standards, automatic generation of test patterns, and consideration of testability issues earlier in the design process.
- Focus on cost of test will give a better understanding of the trade-offs between test methodologies and fault models.
- Throughput will be increased through the use of DFT techniques such as DFT that will allow for the testing of multiple cores in parallel (ADC, DAC, digital, memory).
Any Questions?