## **ISim Testbench Tutorial**

ISIM or the ISE Simulator allows you to analyze and debug your code. This tutorial will show you how to write a simple testbench for your module and run the simulation using ISim.

**1.** First open your project with the top level module that you want to test.



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Design ↔ □ 🗗 X 🗧 7 // Design Name:	~
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Hierarchy 9 // Project Name:	
latch 11 // Target berlines:	
C A K X25500e-fr2an 12 // Description:	
Vers nand New Source 13 //	
Add Source 14 // Dependencies:	
Add Copy of Source 15 //	
Manual Compile Order 17 // Revision D.D.1 - File Created	
18 // Additional Comments:	
Implement Top Module     19 //	
File/Path Display         20         ////////////////////////////////////	
21 module nand_latch(	
Chance All 23 input G,	
No Processes Ru 24 Output q,	
W horized doin man (A) Find Ctrl+F 25 output q_bar	
1 US single design mode and the single design Properties 26 );	
Designed an observation 27	
30 always 8 (d or set)	
31 if (set == 1) begin	
32   q = d;	
$q_{\text{bar}} = -d;$	
34 end	
36 Entimodale	
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	>
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Add a new source to the project	Ln 20 Col 83 Verilog

2. Next we need to create the testbench for this design. Add a new source to the design

**3.** Select Verilog Module and name your testbench.

🔤 New Source Wizard	
Select Source Type Select source type, file name and its location.	
BMM File         ChipScope Definition and Connection File         Implementation Constraints File         IP (CORE Generator & Architecture Wizard)         MEM File         Schematic         User Document         Verilog Module         Verilog Test Fixture         VHDL Module         VHDL Library         VHDL Package         WHDL Test Bench         Embedded Processor	File name:   nand_latch_test    Location:   C:\Code\latch
More Info	Next > Cancel

**4.** The testbench does not require any inputs or outputs so you can ignore the ports window.

Define Mo Specify	dule • ports for module.						
1odule name	nand_latch_test						
	Port Name	Direction Bu		Bus	MSB	LSB	13
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**5.** This is what your project window should look like after adding your testbench.

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Console		+ □ ₽ ×
<pre>UINFO:ProjectMgmt:656 - Parsing desi Started : "Launching ISE Text Edito" </pre>	<pre>in hierarchy completed successfully. t to edit nand_latch_test.v".</pre>	~
Console S Errors 🔬 Warnings 🕅 Find in	Files Results	Ln 1 Col 1 Verilog



**6.** Next create your testbench. After you save it your project should look like this.

**7.** Inside the design area select the simulation radial button (circled in red). Select your testbench and double click simulate behavioral model.



**8.** ISim will launch and from here you can look at your waveform to debug your top level module. Anything set to display to the console will be saved in "isim.txt" in your project folder.

