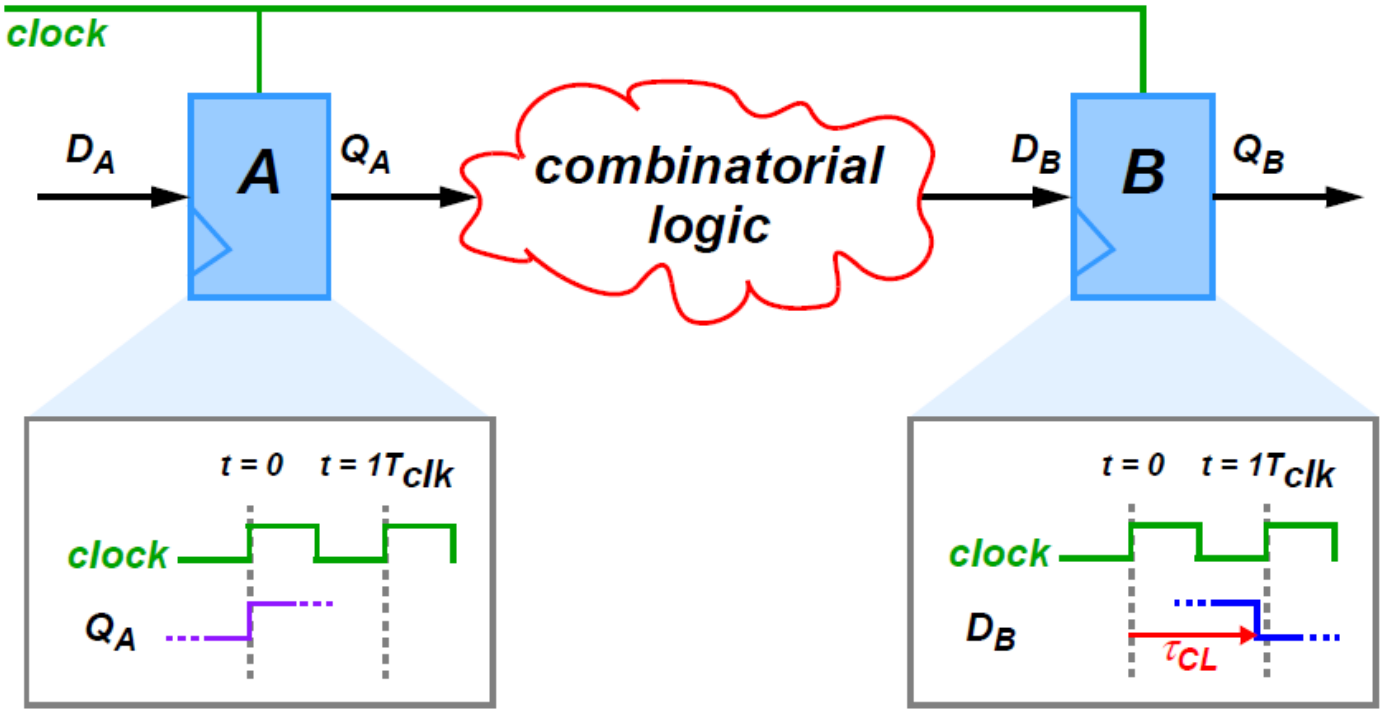
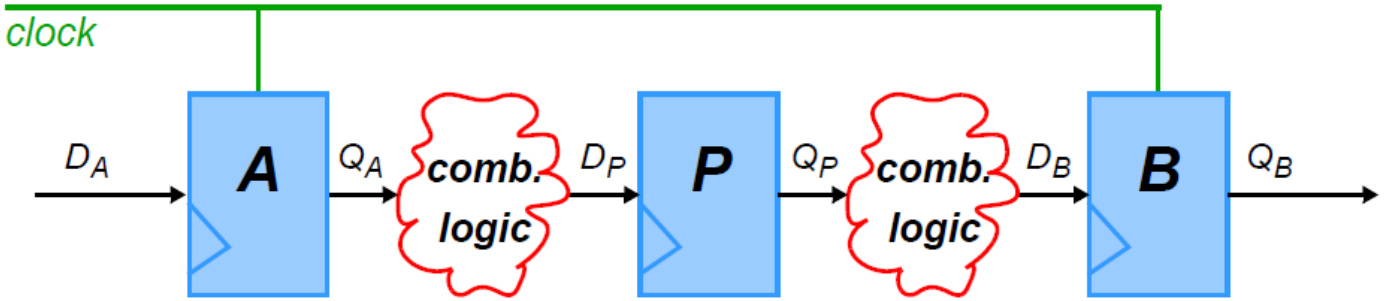
Critical Path and Clock Frequency

- A key performance indicator of FPGA designs is the maximum clock frequency at which they will operate.
- This is limited by the longest propagation delay along a combinatorial logic path between two clocked elements (the ***critical path***).



Pipelining and Latency

- Having noted the dependence of clock frequency on length of combinatorial logic path, we might seek to break this up by inserting additional registers. This process is referred to as ***pipelining***.
- To continue the previous example, we insert the register ***P***, and divide the combinatorial logic path into two equal sections.



- The effect of adding the additional ***pipeline*** register is to increase the maximum clock frequency by a factor of 2.
- However a less desirable consequence is to delay the output by one clock cycle (i.e. add 1 clock cycle of ***latency***).